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RELIABILITY OF SOLID STATE INTEGRATED CIRCUITS

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RELIABILITY OF SOLID STATE INTEGRATED CIRCUITS

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[Book by Ivan Yefimovich Yefimov, Igor' Georgiyevich Kal'man and Vladimir Ivanovich Martynov: "Hard Integrated Circuit Reliability; Second Edition, revised and supplemented", Izdatel'stvo standartov, 15,000 copies, 216 pages]

CONTENTS

Annotation

The major aspects of semiconductor integrated circuit (IC) reliability are treated in the book. The kinds and main reasons for IC failures during the production process and in operation are cited. Methods of quality control as well as the estimation and prediction of IC reliability are analyzed.

The book is intended for engineering and technical workers engaged in the production and utilization of semiconductor IC's, and will also be useful to students in the VUZes and technical schools for the appropriate specialties. There are 31 figures, 26 tables and 186 bibliographical citations.

Table of Contents [Original pagination]

Chapter I. Basic Concepts of Semiconductor Integrated Microcircuits

A semiconductor integrated microcircuit takes the form of an electronic circuit produced in a monolithic semiconductor chip. The various regions of the chip function as independent active or passive circuit components, which are coupled together by a system of thin film conductors. Such a monolithic circuit, as a rule, is enclosed in a hermetically sealed package, where the electrical connections between the contact areas of the circuit on the chip and the package leads are usually made with gold or aluminum conductors.

Modern technological methods, used for the construction of IC's, make it possible through the use of the properties of semiconductor materials to fabricate both the active components (transistors, dipoles) and the passive components (resistors, capacitors) of the circuit in the volume and on the surface of a single chip. The techniques of epitaxial build-up of semiconductor material layers, photolithographic etchings, dopant impurity diffusion, oxidation, thin film deposition and other technologies are employed for these purposes.

Certain IC components are depicted schematically in Table 1 which are produced by planar epitaxy with insulation using p-n junctions. Various combinations of active and passive components are used to realize monolithic IC's for various functional purposes.

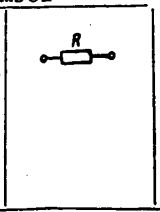
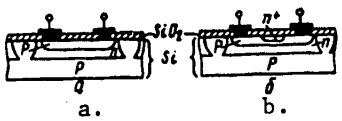
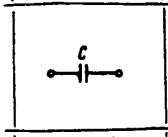
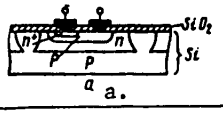
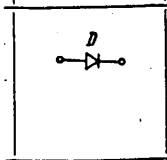
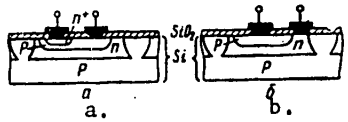
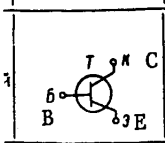
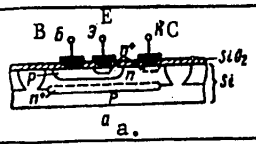
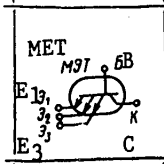
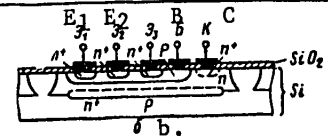
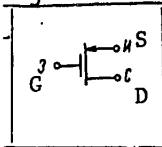
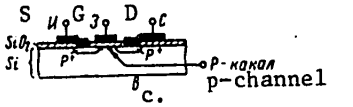
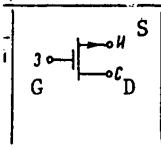
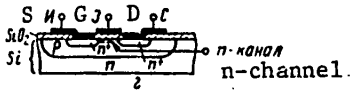
From a structural standpoint, IC's have come to be conventionally broken down into two classes. The first class is logic or digital circuits, which are used basically in digital computers and controllers [1, 2, 4]. In an integrated circuit design, the circuits of this class are realized both in the form of individual logic elements (gates) of the following types: "NAND", "NOR","NAND/NOR", etc., as well as in the form of more complex elements (flip-flop, buffer circuits, half-adders, counters, etc.).

The second class IC's is comprised of linear or analog circuits. These include primarily different kinds of amplifiers (multistage, differential, operational, video amplifiers, read amplifiers, analog switches, etc.). It is more difficult to make such microcircuits in integrated circuit form. The reason for this consists in the lack of integrated circuit inductive components and in the high requirements placed on the precision of IC resistors.

The major advantages of linear integrated circuits as compared to analog circuits using discrete components are the improved temperature stability (related, in particular, to the identical nature of the characteristics of planar transistors), as well as the favorable capability of realizing negative feedback. This is responsible for the high operational reliability of linear IC's.

There is yet another class of integrated circuits which takes the form of a unique "hybrid" of integrated circuits of the first two classes. These are linear pulse IC's, which usually include various current drivers. Logic gates are inserted at the input to these IC's (for example, TTL circuitry), while analog current pulse drivers with a high power dissipation level are inserted at the

TABLE 1.

Designation of the Circuit Component	Conventional Symbol	Schematic Depiction of the Component Fabricated with Solid State Technology
1. Resistor: a) Simple; b) Diffusion "pinch";		
2. Capacitor		
3. Diode using emitter and collector p-n junctions		
4. Transistor: a) Simple n-p-n bipolar		
b) Multiple emitter bipolar;		
c) p-channel MOS		
d) n-channel MOS (complementary)		

output. The production technology for linear pulse IC's does not differ from the technology used in the fabrication of logic and linear IC's.

We shall treat in somewhat more detail the first class of microcircuits. The following logic gates have become the most widespread at the present time [1, 3-6]:

--Resistor transistor or current switching circuits (PTTL), and MOS transistors of the same type of conductivity.

The increase in the functional complexity and level of integration of integrated semiconductor circuits required the modification of existing circuit designs and the creation of new ones which make it possible to substantially improve the characteristics of the basic logic elements and large scale integrated circuits (LSI's), designed around them (reduction in the power dissipation, increase in the circuit speed, reduction in the area of the basic logic gates, etc.). As a result, such logic circuits as the following are being developed and placed in production [10-15]:

--Modified transistor logic (with a supplemental transistor in the output circuit): T^3L;
--Integrated injection logic: I^2L;
--Emitter follower logic: EFL;
--Logic using complementary MOS transistors: CMOS;
--Logic using charge coupled devices: CCD's, etc.

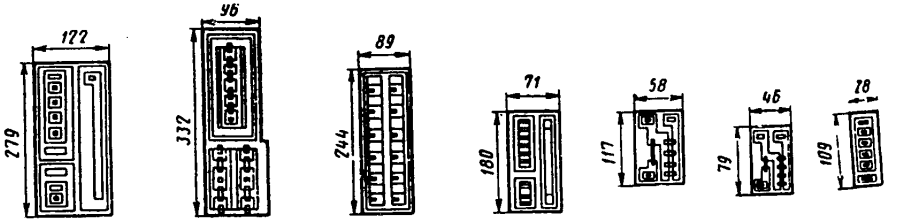
Logic circuits are most easily realized in integrated circuit form. Because of the fact that the logic devices (modules, assemblies) of electronic digital computers (ETsVM) can be put together from identical functional components, the finite series of logic IC's needed for computer construction consists of a comparatively small number (5 to 20) of standardized circuits. The use of IC's as digital computer components which, as a rule, operate in the milliwatt and microwatt power ranges, improves their operational reliability. This, in particular, has been responsible for the predominant development of logic IC's as compared to linear ones.

The constant striving towards microminiaturization of integrated circuits led to the fact that the component layou.. density on a microcircuit chip increased by more than three orders of magnitude over a decade (from 1962 through 1972). In this case, the increased level of integration of IC's was achieved by increasing the chip dimensions (from 1 mm^2 in 1962 to approximately 6 mm^2 in 1973), reducing the average size of the components and the spacings between them on the chip (from $2 \cdot 10^{-2}$ mm^2 in 1962 to $1 \cdot 10^{-3}$ mm^2 in 1973) and using multilevel interconnections, which made it possible to approximately quadruple the ratio of the actually utilized area to the overall area of the IC chip [17].

Component miniaturization became possible only because of the refinement of the fabrication technology processes for IC's and optical production process equipment which makes it possible to use precision photographic templates for quite sizeable areas.

TABLE 2.

Comparative Characteristics of Four-Input Basic Logic Gates Used to Realize Monolithic Integrated Circuits

Топология базового четырехвходового логического элемента (вентиля)* (1)							
Технологическая характеристика Technological Characteristics	Type of Circuit Тип схемы						
	Standard Стандартная ТТЛ—СИС TTL-LSI	КМДП CMOS	ЭСЛ—БИС ECL-LSI	ТТЛ—БИС TTL-LSI	р-МДП p-MOS	n-МДП с кремниевыми затворами (2)	И²Л I^2L
(3) Количество компонентов	3	3	3	3	2	2	1
(4) Площадь вентиля, мм²	0,034	0,032	0,02	0,013	0,007	0,0036	0,003
(5) Количество фотошаблонов	7	6	7	7	4	7	4
(6) Количество диффузионных операций	4	3	4	4	1	3	2
(7) Время задержки на один вентиль, нс	10—25	25—100	1—10	1—10	1000	100	1—10

* Размеры в мкм.
*Dimensions in micrometers

Key: 1. Topology of the basic 4-input logic element (gate)*;
2. n-MOS with silicon gates;
3. Number of components;
4. Circuit area, mm^2;
5. Number of photographic templates;
6. Number of diffusion operations;
7. Delay time per logic gate, nsec.

As a result of working out the engineering design solutions and the fabrication technologies for logic integrated circuits, considerable progress was achieved in the field of microminiaturization of electronic systems. Individual printed circuit boards with logic IC's, combined in the modules and assemblies of digital computers, are being replaced at the present time by series and random access memories (ZU), logic gates with an arbitrary structure and microprocessors, made on individual chips, i.e., realized in the form of LSI's [10].

The basis for the achievements in the field of systems engineering is the extensive set of technologies, which are distinguished by their diversity and capabilities of improving the qualitative characteristics of IC components.

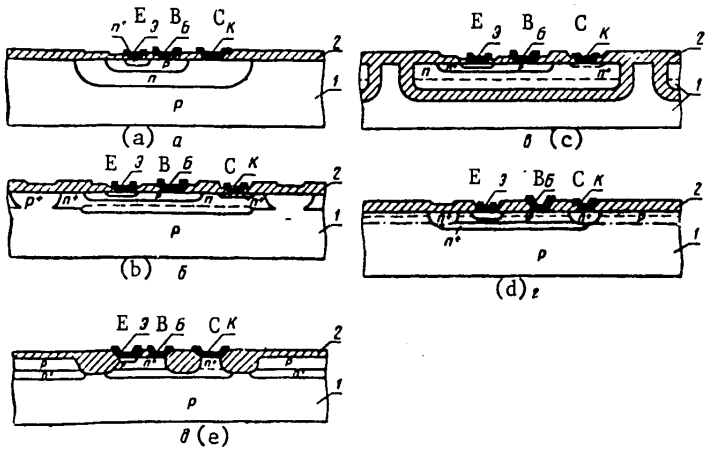


Figure 1. (a-e). Transverse sections through planar transistor structures, fabricated using various technologies.

Key: 1. Silicon;
2. Silicon dioxide;
a. Triple diffusion (3 D technology);
b. Epitaxial collector (planar epitaxial technology with insulation of the elements by p-n junctions);
c. With dielectric insulation;
d. Insulation created during collector diffusion (CID technology);
e. Isoplanar technology (with insulation of the elements by a dielectric).

The topological drawings and technological characteristics of various four-input basic logic gates, realized in the form of TTL, ECL, I^2L and MOS structures are shown in Table 2 to compare the capabilities of the various technologies [11,12].

The maximum functional density (number of circuit functions per unit of chip area) is limited by the amount of power dissipation or the area occupied by the transistors, interconnections and passive elements [9]. Thus, the maximum packaging density of an IC is obtained with a minimization of the supply voltage and

the geometric dimensions of its components. Since the minimum size of the major IC element (transistor) is governed by the "closure" effect (the mutual overlapping of depleted layers when the supply voltage is raised), to further reduce IC dimensions, it is necessary to increase the doping concentration of the diffusion regions of the structures with fine layers.

Cross-sections through planar transistor structures fabricated using various technologies are shown schematically as an illustration in Figure 1 (a-e):

--Triple diffusion (3 D technology) (Figure 1 a);
--Insulation created during collector diffusion (CID technology) (Figure 1 d);
--Isoplanar technology (with the insulation of the elements by a dielectric) (Figure 1 e).

The technologies for fabricating integrated semiconductor circuits have been treated in detail in domestic and foreign literature [7, 2, 4, 5, 8]. For this reason, in this section we will deal with questions of IC fabrication technology only in order to discuss the major factors governing their reliability.

Planar technology methods are used to construct IC's (doping impurity diffusion, plate oxidation and photolithographic etching of an oxide film, thin film deposition, etc.), which make it possible to obtain individual circuit components and make electrical connections between the components by means of thin film conductors ("metallization"). A combined technology is used when fabricating resistors with high nominal values and having a small scatter in their characteristics. A distinctive feature of combined technology is the fabrication of resistors by means of deposition on the surface of the semiconductor structure, created by planar epitaxy, of a thin film of material with a high specific resistance.

Silicon usually serves as the main semiconductor material used in the fabrication of IC's. The use of silicon assures good producibility of the devices in the fabrication process using planar technology methods. In this case, the execution of the oxidation and photolithography operations on silicon is substantially simpler than when other semiconductor materials are used. Moreover, the operational temperature range of semiconductor devices made from silicon is significantly wider than for germanium devices. However, the merits of silicon do not preclude the possibility of using other raw materials in some cases.

We shall consider one of the basic technological processes in the fabrication of IC's using planar epitaxy with insulation of the elements by p-n junctions and one-level metallization.

A chip of p-type silicon with an epitaxially grown layer of n-type silicon on it and locally formed hidden n^+ type layers, located at the "epitaxial film--substrate" separation boundary in the regions of the future transistors of the IC's for the purpose of improving their electrical parameters serves as the starting material in this case.

Using group techiques, by means of alternate oxidation, photolithography, diffusion and deposition operations, several hundreds of chips are produced simultaneously on this plate, where each of the chips takes the form of a complete

microcircuit. After this, the plate is cut into individual chips and each chip is mounted in a package. Then the packages are hermetically sealed and the quality control and sorting of the finished IC's are carried out.

Cross-sections through such an IC in various stages of the technological process of its fabrication are shown schematically in Figure 2 (a-f). For the sake of simplicity, only the transistor structure and diffusion resistor are shown. Diodes, as has been noted, are realized on the basis of the transistor structure by using its individual junctions ("emitter-base" or "collector-base"). The typical production process consists of the following main operations:

--Oxidation of the plates of the starting material (Figure 2a);
--Photolithographic etching of the oxide film to produce the configuration of the insulated regions:
--Stage I of boron diffusion (infusion - the application of the boron);
--Stage II boron diffusion (dispersal - the insulating diffusion of the boron through the entire thickness of the epitaxial layer) and oxidation of the silicon (Figure 2b);
--Photolithographic etching of the oxide film to create "windows" underneath the base regions of the transistors and underneath the diffusion resistors;
--Stage I boron diffusion (application of the boron to the surface of the bases and resistors);
--Stage II boron diffusion (dispersal of the dopant to the requisite doping depth of the base--collector junction) and the oxidation of the silicon in the "windows" (Figure 2c);
--Photolithographic etching of the oxide film to create "windows" underneath the emitter regions and the contact areas of the collector;
--Stage I phosphorus diffusion (application of the phosphorus to the surface of the emitter areas and the collector contacts);
--Stage II phosphorus diffusion (dispersal of the dopant to the requisite doping depth of the emitter--base junction) and the oxidation of the silicon in the "windows" (Figure 2d)*;
--Photolithographic etching of the oxide film to create "windows" underneath the contacts (Figure 2e);
--Deposition of a thin aluminum film;
--Photolithographic etching of the aluminum to shape the requisite configuration of the internal circuit wiring between the components (Figure 2f);
--The melting-in of the aluminum;
--The cutting of the plates into chips;
--Sorting and rejection of the chips (finished IC structures) with respect to the electrical characteristics as well as visually;
--Mounting of the chip on the package base;
--Heat compression or ultrasonic welding of wire leads to the contact areas on the chip;
--The welding of the wire leads to the external package leads;
--The hermetic sealing of the IC;
--Technological testing of the IC;
--Sorting and rejection of the IC's with respect to the parameters.

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*The stage I and II phosphorus diffusion operations can be combined in a single process.

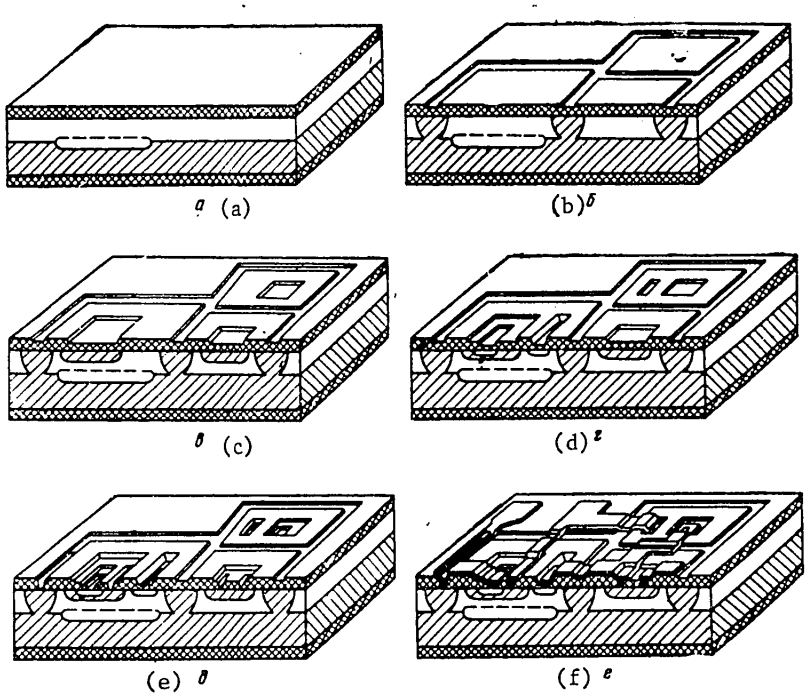

Figure 2 (a-f). Schematic depiction of the cross-sections of an integrated circuit at various stages in the fabrication.

The oxidation of the plate is accomplished in an oxidizing atmosphere at high temperature. The thickness of the layer should be sufficient so that with subsequent diffusion operations, the penetration of the diffusant into the oxidized regions of the silicon plate is prevented and reliable protection of the surface of the already fabricated structure is assured.

The photolithographic etching of the oxide film as well as the diffusion of the doping impurity and the oxidation of the silicon must be handled separately, since the sequential alternation of these main processes makes it possible to essentially obtain the entire structure of the circuit and assure the requisite internal circuit layout separation.

The function of the photolithography process consists in shaping the "windows" in the oxide film, which are intended for the diffusion of the doping impurities or for the fabrication of contacts to the silicon in regions of the plate cleaned of oxide, as well as for making internal circuit connections (interconnections) of a definite configuration between the individual components of the integrated circuit.

For this purpose, a thin layer of photosensitive varnish, the photoresist, is applied to the oxidized surface of the plate, after which the figure is

transferred from the photographic template to the photoresist layer by means of contact or projection photographic printing. Ultraviolet irradiation of the photographic layer increases the speed of photoresist dissolution in the developer. During the developing process, the exposed portions of the photoresist are dissolved in the developing solution. After thermal hardening - the polymerization of the remaining photoresist - an acid resistant mask is obtained, which makes it possible to etch the oxide (or metal) film in the areas not protected by the photoresist, and thereby obtain in the oxide (or metal) film the figure corresponding to the photographic template. When the oxide etching process is completed, the plate is cleaned of the photoresist, after which the plate with the corresponding figure in the oxide is sent on for the doping impurity diffusion operation (or the operation of melting in metal). The diffusion of doping impurities is intended to create regions of p or n conductivity at the appropriate points in the chip. The doping impurities diffused into the chip at points free of the oxide, which makes it possible to localize the impurities in the corresponding regions of the semiconductor material and thereby create the requisite circuit components.

For the purpose of having better control of the diffusion process, it is usually accomplished in two stages. The impurity is initially applied to the surface of the plates, which then goes into the shallow surface layer of the silicon through the "windows" in the oxide (Figure 3). After this, the plates are annealed at high temperature in an oxidizing gas medium, the so-called dispersal of the impurity. In this case, the impurity diffuses down to a specified depth, producing the requisite diffusion profile, while the oxide film which appears protects the surface of the plate and the p-n junction being created against exposure to the environment.

We shall now analyze the process of fabricating a silicon IC step by step.

After the oxide film is applied to the plate of the original silicon, it is photolithographically etched to produce the configuration of the insulating regions. As as result, grooves are created in the oxide film which expose the silicon for the diffusion of the p-type doping impurity in these regions, something which is essential for the creation of electrically insulated n-type "pockets", in which the individual integrated circuit components will be fabricated in subsequent stages (Figures 3a, b).

Windows underneath the base regions and underneath the diffusion resistors are created in the second photolithographic stage in the corresponding insulated portions of the structure. The resulting figure on the oxide film should precisely match the relief obtained as a result of the first photolithography.

The next diffusion of the p-type doping impurity is necessary to produce the base collector junctions and the regions of the diffusion resistors. The holes created in the oxide by the preceding photolithographic etching are covered with an oxide layer, which is grown thermally during the second stage of boron diffusion (Figure 3c).

In the subsequent step, the third photolithographic etching is accomplished for the purpose of creating "windows" underneath the emitter regions and the

contact areas of the collectors. It is absolutely necessary in this case that the new pattern of the photographic template completely match the already existing pattern on the oxide layer.

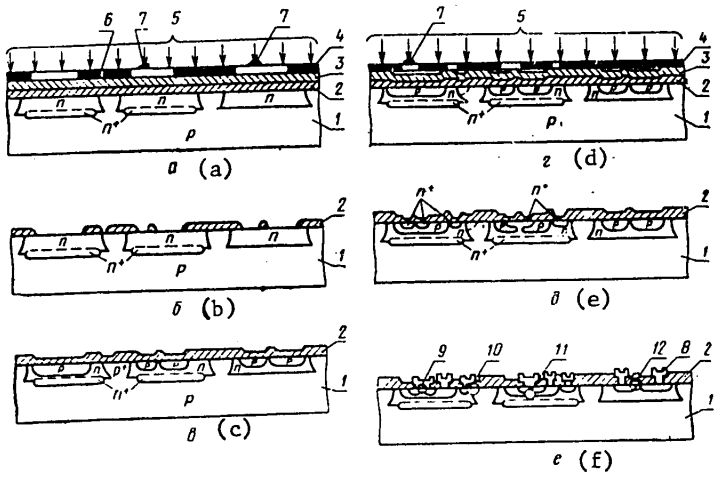

Figure 3. Defects in integrated circuits related to photolithography defects.

Key:
1. Silicon;
2. Silicon dioxide;
3. Photoresist;
4. Photographic template;
5. Ultraviolet radiation;
6. Scratch on the photographic template;
7. Dust particle;
8. Aluminum;
9. "Base-emitter" short circuit;
10. p-n junction with low breakdown voltage;
11. "Emitter-collector" short circuit;
12. Diffusion tube, diffusion resistor break.

The next phosphorus diffusion produces n-type regions needed for making the emitters of planar transistors and the regions of contacts to the collectors, which makes it possible to improve the characteristics of the corresponding ohmic contacts (Figures 3d, e).

Then the fourth photolithographic etching is carried out, during which "windows" are created in the oxide underneath the contacts to all elements of the planar structure formed during the preceding operations in the production process cycle.

After this, the internal circuit connections are made between the individual components (Figure 3f). For this purpose, an aluminum layer is initially

deposited on the entire surface of the plate, and then by means of photolithography the unnecessary aluminum is removed, as a result of which, the requisite pattern of connections between components is produced. The operation of melting in the aluminum promotes an improvement in the adhesion (sticking) of the metal film to the surface of the substrate, as well as an improvement in the characteristics of the ohmic contacts. At this stage, the production process for producing the structure of the integrated microcircuit is essentially completed. Subsequent operations, as has already been noted, are carried out to break the plate up into chips, mount the chips in packages, hermetically seal the packages and check the characteristics of the finished IC's.

To realize all of the advantages of semiconductor microelectronics which assure a high level of IC quality and reliability while maintaining a high percentage of good product output, careful handling of all of the technological operations and the assurance of effective monitoring of the IC production process are essential. This is especially important in the production of integrated circuits with an increased level of integration. The task is facilitated significantly by the fact that the technological operations and the equipment used are of the same type, which makes it possible, first of all, to standardize the production process using a limited number of basic technological processes for IC fabrication, and secondly, to provide for effective control of the production process and thereby achieve high IC quality and reliability.

The following play a large role in IC production: the purity and perfection of the crystalline structure of the semiconductor materials; the careful processing of the plates, which provides for high purity of their surface; the use of ultrapure chemicals, water and gases; high photographic template quality (strict tolerances for the geometric dimensions, no damage to the pattern of the photographic layer and "compatibility" of the set); and precision in the combining operations.

All of these requirements follow from the major feature of the production of integrated circuits with a high layout density of the circuit components on a single chip. If only one dust particle of micron size or diffusant particle gets on the surface of a planar structure during the diffusion (Figure 4a), oxidation (Figure 4b) or photolithography, it can lead to the disruption of the requisite diffusion profile and the appearance of so-called "diffusion tubes" or to a degradation of the oxide film quality (punctures, holes), which serve as the cause of short circuits, elevated leakage currents and a reduction in breakdown voltages.

The presence of dirt and moisture in the energy vehicles, for example, in the oxidizing or inert gases, has a negative impact on IC quality, since the masking and passivating properties of the oxide film are sharply degraded in this case, something which, in the first place, significantly reduces the output percentage of good circuits, and secondly, can lead to the most diverse IC failures during their testing and operation.

Dislocations, microcracks, sections with a nonuniform doping impurity distribution and other microdefects in the crystal lattice of the initial semiconductor

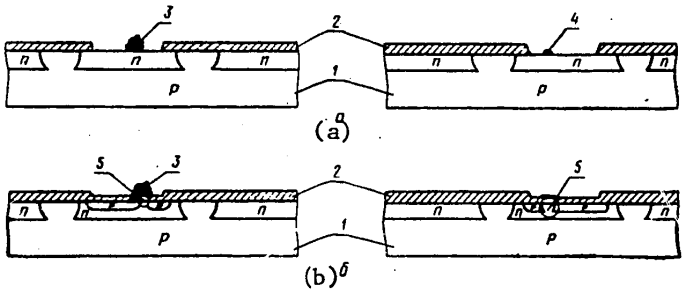

Figure 4. Defects in integrated circuits related to diffusion defects.
Key: 1. Silicon;
2. Silicon dioxide;
3. Dust particle;
4. Diffusant (donor) particle;
5. Diffusion tube, diffusion resistor break.

material are causes of the appearance of potentially unreliable integrated circuits, especially in the case where the indicated defects occur in the region of the active components of IC's or prove to be close to the p-n junctions.

The precision in combining the templates in the photolithography process, which is due to the great layout density, is of exceptional importance in the production of IC's. If a useful output of 0.85 to 0.9 is obtained after each superimposition operation, then following the fourth combination photolithography process, the quantity of rejects because of just one unsatisfactory combining operation will amount to 35 to 50 percent (in practice, this quantity will be less since several defects occur in the same structure).

It should be noted that when fabricating the contact connections, a whole series of difficulties come up, which are related, first of all, to the complexity of producing intersecting connections, and secondly, to the appearance of parasitic capacitances between thin film conductors positioned close together, the length of which can reach a significant value in complex circuits.

One of the most important problems which occur in IC production is the problem of insulating circuit components. The choice of the method of insulation plays a substantial part from the viewpoint of both the fabrication technology and the quality and reliability of the finished IC's, since the insulation determines the parasitic feedback loops (leakages, parasitic capacitances, etc.) between the circuit elements. The method of insulating elements with isolating p-n junctions was described above. Other techniques of element insulation are also possible, for example, using a layer of silicon dioxide.

The design of high quality and high reliability IC's is a complex problem. The fabrication technology for IC's gives them advantages over semiconductor devices

and other electronic technology products. However, these advantages can be realized only given the condition that all of the specific features of IC production are carefully taken into account and with the comprehensive resolution of several structural design and technological problems.

Chapter II. The Reliability of Semiconductor Integrated Circuits

In integrated semiconductor circuits, the active and passive components are combined in a monolithic chip and manufactured in a single technological process. This is responsible for their high liability [1, 2, 4, 18, 19].

Planar technology is employed in the fabrication of IC's, which provides for good protection of the p-n junctions against the impact of the environment. Microcircuits, as was noted in Chapter I, are fabricated using a group technique, in which several hundreds of semiconductor IC chips are produced on one plate of semiconductor material under identical conditions and production modes. The hermetic sealing of the finished functional unit, which is the integrated circuit, in a single package makes it possible to simultaneously protect the entire set of circuit components against exposure to the environment. It is anticipated in this case that the reliability of a circuit enclosed in a single package will increase with increasing circuit complexity and number of components, figured on a per function basis.

The comparatively small quantity of standard technological operations, the continuity and closed nature of the fabrication process for integrated circuits, within the bounds of a single production line, allow for the maximum automation of the fabrication and quality control processes, a reduction in the probability of allowing errors and the achieving of uniformity in product quality. As compared to semiconductor production, well organized integrated circuit production is characterized by a smaller scatter in the parameters and characteristics of the finished product.

The relatively small number of contact connections in integrated circuits as compared to circuits designed around discrete semiconductor devices and other electronic hardware components, and the more sophisticated fabrication technology for integrated circuits are also responsible for the high reliability of the solid state devices.

Thus, integrated circuit reliability proves to be approximately equal to the reliability of a single transistor, meeting the most modern requirements, while the application of IC's opens up broad possibilities for further improving equipment reliability. Comparative data on the reliability of several radioelectronic assemblies, constructed using various components, are given in Table 3 [20]. An analysis of these and other data makes it possible to draw the conclusion that in the integrated circuit variant, the radioelectronic assemblies have a reliability which is two to three orders of magnitude greater than the reliability of similar devices designed around vacuum tube and semiconductor devices.

It should also be noted that the increase in the functional complexity and level of integration of IC's, related to the increase in the number of components in one device, up to a known limit (up to the level characteristic of circuits using discrete components) does not reduce its reliability. Thus, for example, if the failure rate at normal temperature is 10^{-7} hr^{-1}, and at a

TABLE 3. Comparative Data on the Reliability of Radioelectronic Equipment Assemblies Constructed Using Various Components (Failure Rate in hr^{-1})

Radioelectronic Equipment Unit (or Device)	Vacuum Tubes	Discrete Semiconductor Device Components		Integrated Circuit
		Ordinary Acceptance Testing	Following Special Selection	
Flip-flop	$5.1 \cdot 10^{-4}$	$5.3 \cdot 10^{-5}$	$3.7 \cdot 10^{-6}$	$8.5 \cdot 10^{-7}$
Half-adder	$4.7 \cdot 10^{-4}$	$3.9 \cdot 10^{-5}$	$1.7 \cdot 10^{-6}$	$8.5 \cdot 10^{-7}$
"NAND" gate	$4.4 \cdot 10^{-4}$	$3.9 \cdot 10^{-5}$	$2.4 \cdot 10^{-6}$	$8.5 \cdot 10^{-7}$
J-K Flip-flop	$9.2 \cdot 10^{-4}$	$9.5 \cdot 10^{-5}$	$4.1 \cdot 10^{-6}$	$8.5 \cdot 10^{-7}$

temperature of +85° C is equal to $6 \cdot 10^{-7}$ hr^{-1} (which corresponds to the reliability of a series produced plan-r silicon transistor) for a microcircuit, equivalent to a radioelectronic circuit consisting of 20 discrete components, then a radioelectronic circuit incorporating 10 such transistors and other components will have a failure rate λ of $(1--6) \cdot 10^{-6}$ hr^{-1}. This clearly illustrates the advantages of semiconductor IC's as components for equipment.

Besides the considerable reduction in the number of components, with the use of IC's in equipment there is a substantial reduction in the number of different kinds of connections, something which also leads to a reduction in its failure rate.

As is well known, contact connections have an impact on the reliability of any device. This is explained by the fact that device or equipment reliability is composed of the reliability of the elements comprising the device or equipment, as well as their connections. For the case of independent failures, this function is written in the following expression:

$$\lambda_{total} = \sum_{i=1}^{k} N_{ei}\lambda_{ei} + \sum_{j=1}^{l} N_{cj}\lambda_{cj}$$

where λ_{total} is the integrated circuit (radioelectronic equipment unit) failure rate;

λ_{ei}, λ_{cj} is the failure rate of the i-th integrated circuit (or device) component and that of the j-th contact connection between the components;

N_{ei}, N_{cj} is the number of components incorporated in the integrated circuit (or the electronic equipment unit), and the number of connections between them.

It is apparent that the use of IC's leads to a sharp reduction in the number of welded and soldered connections between various components, figured on the basis of the function performed.

It is specifically for this reason, that despite the fact that welded contact connection reliability is usually less than the reliability of other structural

elements of monolithic IC's, by virtue of the smaller number of contact connections per unit function which is performed, the reliability of IC's as a whole is better than the reliability of similar electronic products for a similar functional purpose, designed around other components.

For the same reason, the reliability of radioelectronic equipment units designed around IC's is several orders of magnitude higher than the reliability of equipment designed around discrete semiconductor devices, and the "gain" from the use of IC's increases with their increasing level of integration and functional complexity.

An important factor which has a favorable influence on the operational characteristics and reliability of IC's is their low weight. This is due, on one hand, to the good mechanical qualities of both the IC's themselves and the equipment designed around IC's (strength and immunity to the impact of vibration, shock and linear loads). On the other hand, the miniature dimensions (and low power consumption) create the prerequisites for improving radioelectronic equipment reliability by virtue of providing for redundancy.

An finally, the use of IC's as the component base for radioelectronic equipment reduces by many times the possibility of decreasing equipment reliability, related to the incorrect use of the components. This possibility is due primarily to just the technical clarity of the use of integrated circuits. The more discrete electronic products are replaced by IC's, the lower the probability of making mistakes when installing and aligning equipment.

In step with the refinement of the structural design of IC's, their fabrication technology as well as the accumulation of experience with the manufacture and operation of radioelectronic equipment designed around IC's, a substantial improvement is being observed in the quantitative indicators for the production and operational reliability of IC's.

The IC reliability level achieved at the present stage of integrated circuit electronics development is characterized in different cases of IC applications by a nonfailure operating probability of 0.999 - 0.9999 in 10,000 hours. According to some data obtained from the sphere of radioelectronic equipment operation, the failure rate of IC's is $7 \cdot 10^{-9}$ hr^{-1} at a confidence level of 0.6 [21, 27, 28].

The service life of solid state semiconductor devices is significantly greater than the service life of other electronic equipment products. At the present time, accepted practice is to guarantee a service life for IC's of 10,000 to 15,000 hr. An improvement in the quality of the package protection for IC's, an increase in the reliability of their contact connections up to the level of the reliability of the semiconductor structures, a further increase in the quality of the active elements and the stability of the surface properties of planar structures as well as the absolute observance of the requirements of the technical specifications and standard setting documentation during operation will make it possible to achieve the ultimately possible service life and reliability of IC's.

TABLE 4. Generalized Data on U.S. Integrated Circuit Reliability

Conditions	Temperature °C	Volume of the tests, x 10^7 circuit-hr	Maximum value of the failure rate for a confidence level of 0.6 and higher, hr^{-1}
IC operation as part of radioelectronic equipment	--	More than 35	$(0.7--90) \cdot 10^{-8}$
Service life tests of IC's	25	More than 1	$(0.6--6.7) \cdot 10^{-7}$
Operation of minicomputers using MOS LSI	55	About 5	$0.8 \cdot 10^{-7}$
Service life tests of IC's	85--125	More than 7	$(0.16--18.0) \cdot 10^{-6}$
The same	125	More than 1.1	$8.4 \cdot 10^{-8}$
The same	125	About 4.3	$2.2 \cdot 10^{-8}$
The same	150--200	More than 0.6	$(0.02--5.0) \cdot 10^{-5}$
Field tests	--	More than 0.5	$1.8 \cdot 10^{-6}$
Accelerated stepped tests	125--200	More than 0.9	$6 \cdot 10^{-6}$
Storage	25	More than 1.7	$5.6 \cdot 10^{-8}$
The same	150	More than 9	$0.63 \cdot 10^{-7}$
The same	150--175	More than 3	$(2.2--2.9) \cdot 10^{-6}$
The same	200--300	More than 1	$(0.9--2.4) \cdot 10^{-5}$

Generalized data on IC reliability, obtained from tests of IC's and during operation of radioelectronic and other equipment and instruments using these components, are given in Table 4 [20-28, 30]. And the curves shown in Figure 5 demonstrate the reduction in the failure rate of semiconductor IC's made by Texas Instruments Inc. during 1961--1973. The reliability of series produced products has grown by several orders of magnitude over the past decade. As far as microcircuits produced in accordance with special programs for particularly important facilities are concerned, the growth in their reliability is characterized by even more impressive figures [27].

The convincing success in achieving the high "natural" reliability inherent in solid state components gave the specialists of the above mentioned company the incentive to intoduce a new measurement unit for the integrated circuit failure rate into everyday practice. Since in operating with the measurement unit adopted in the U.S. for the failure rate - percent per 1,000 hr - with a low failure rate (hundredths and thousandths of a percent), there is a high probability of erroneously estimating the reliability, a new measurement unit was introduced into practice: the FIT. One FIT is equal to one IC failure per 10^9 device hours [28].

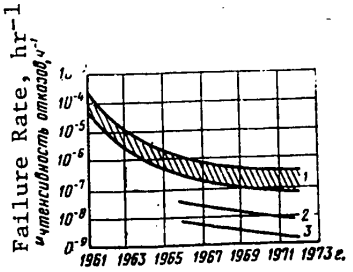

Figure 5. The decrease in the failure rate of IC's

Key: 1. Series production;
2,3. Integrated circuits fabricated in accordance with various reliability programs.

In analyzing the data of the table, the conclusion can be drawn that the reliability of IC's incorporated in electronic equipment when it is in operation is considerably higher than their reliability determined during testing.

This is explained by the fact that during operation, IC's usually operate in less severe modes than during the testing process. A properly designed radioelectronic system provides for its components to be used in alleviated operating modes and in the majority of cases, under conditions close to normal. The electrical circuits of such systems are designed taking into account the permissible variations in the values of the major parameters. A circumstance of no small importance is also the massive numbers of IC's in service and the long operating time, which are responsible for the accumulation of an enormous amount of experimental material, and consequently, the high statistical significance of the estimate.

When testing IC's though, everything is reversed. In striving for production profitability, reduction in the product manufacturing time and an increased percentage output of good products, the manufacturer directs his efforts primarily towards the timeliness of obtaining data on the quality and reliability of the output product. For this purpose, he knowingly limits the scope of the tests, compensating for this by increasing the severity of the test modes, conditions and evaluation criteria for the test results.

The accumulated operational and testing experience makes it possible to state that inherent in IC's fabricated using planar epitaxial technology is a lack of an explicitly pronounced burn-in period and in practice, a minor and timewise uniform failure of IC's is observed in the process of their long term operation under normal conditions (Figure 6).

At the same time, during tests of IC's under conditions of severe loads (especially with the loads applied in combination), an elevated failure rate of the IC's is observed in their initial period of operation. The potentially unreliable samples, having hidden production defects (and by virtue of this, a short service life), generally fail in a period of 1,000 hours of operation. The majority of them fail in the first 200 to 500 hours. Incorporating special kinds of tests in the production process cycle for IC fabrication provides for the timely rejection of such circuits [4, 20, 27-30] and increases the reliability of the manufactured batches of devices.

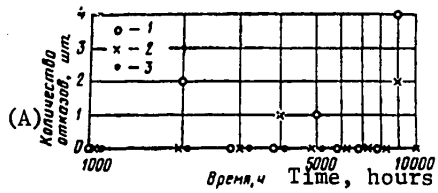

Figure 6. The failure distribution of IC's fabricated using planar epitaxial technology as a function of time for reliability testing at an ambient temperature of +125° C

Key: 1. IC chopper;
2. Micropower "OR--NAND--NOT" IC;
3. Logic IC
A. Number of failures, units.

The electrical load has a substantial impact on IC reliability. With the action of the current flowing through an IC, because of local overheating at defective points in the metalized interconnections (scratches, local thin places in the aluminum film at stepped points in the oxide down to values lower than the permissible) melting of the interconnection material takes place, while in the presence of moisture and dirt, corrosion of the aluminum wires and other thin film components of the IC is observed.

A voltage applied to a device causes the formation of surface channels with the opposite type of conductivity and breakdown of the oxide in samples with a contaminated surface or with an elevated content of metal impurities in the oxide layers.

Under certain conditions, the electrical voltage applied to an IC can lead to the formation of electrical fields which act on the device similar to the action of a mechanical load, localized at one point.

The criticality of IC's to electrical overloads is responsible for the special requirements placed on the use of these devices. The operational modes of radioelectronic equipment and systems using IC's should also preclude the appearance of electromagnetic pulses as well as those transient processes when switching circuits and when defects occur which would cause the IC to fail.

An analysis of the operational data and the results of all possible IC tests shows that the IC failure rate during operation and storage differ substantially and depends greatly on the ambient temperature (Figure 7).

The ambient temperature, along with IC overheating caused by internal power dissipation, leads to a change in device parameters. The transistors of IC's are especially sensitive to a temperature change. Just as significant as the temperature dependence is the temperature coefficient of resistance (TKS). Plotted in Figure 8 are graphs which illustrate some of the major parameters, the properties of IC quality, as a function of temperature [4], and Table 5, the mean time between failures as a function of the junction temperature.

Because of the structural design and production process features of silicon IC's, the impact of temperature on their reliability is a great deal less than on certain other semiconductor devices, in particular, germanium ones, nonetheless it is significant, and this phenomenon cannot be disregarded.

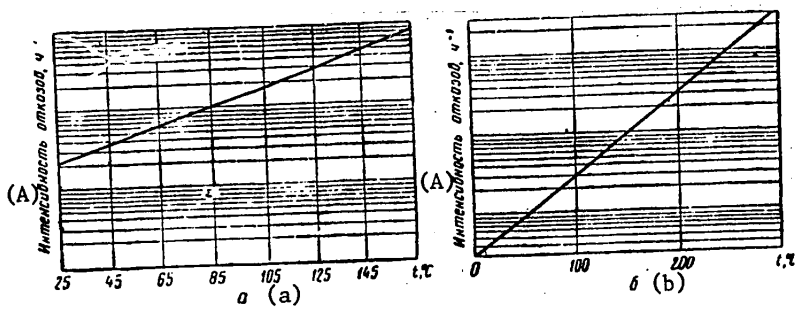

Figure 7. Typical function $\lambda = f(T)$ for IC's during operation (a) and in storage (b).
Key: A. Failure rate, hr^{-1}

Numerous studies have made it possible to establish that parameter instability of a semiconductor structure in IC's occurs as a result of exposure to an elevated temperature at temperatures above 300° C. It can be seen from Figure 9, where the major electrical parameters of a three-input "NOR" logic gate is plotted as a function of the ambient temperature that up to a temperature of +300° C, no substantial changes are observed in the values of the parameters. Only at temperatures above +300° C is a significant deviation noted in the majority of devices in the values of the parameters from the initial values. It is supposed that with exposure to high temperature, leakage channels appear close to the p-n junctions. Along with this, reliability tests of these circuits at a temperature of up to +300° C have demonstrated the high stability of the major electrical parameters (Figure 10).

TABLE 5.

Junction Operating Temperature, °C	Mean Time Between Failures, 24-hr Days
80	6,944
100	1,191
120	243
140	58.5

The following are numbered among the defects which occur with combined exposure to high temperature and electrical loads: the formation of transition metal compounds with increased brittleness and high electrical resistance, the formation of electrical insulating layers at the "aluminum--silicon" separation boundary, corrosion of the aluminum in cracks and at oxide steps, etc.

Among IC failures which occur when they are tested for reliability under conditions of normal and elevated ambient temperatures, catastrophic failures predominate. The bulk of these failures is due to connection defects.

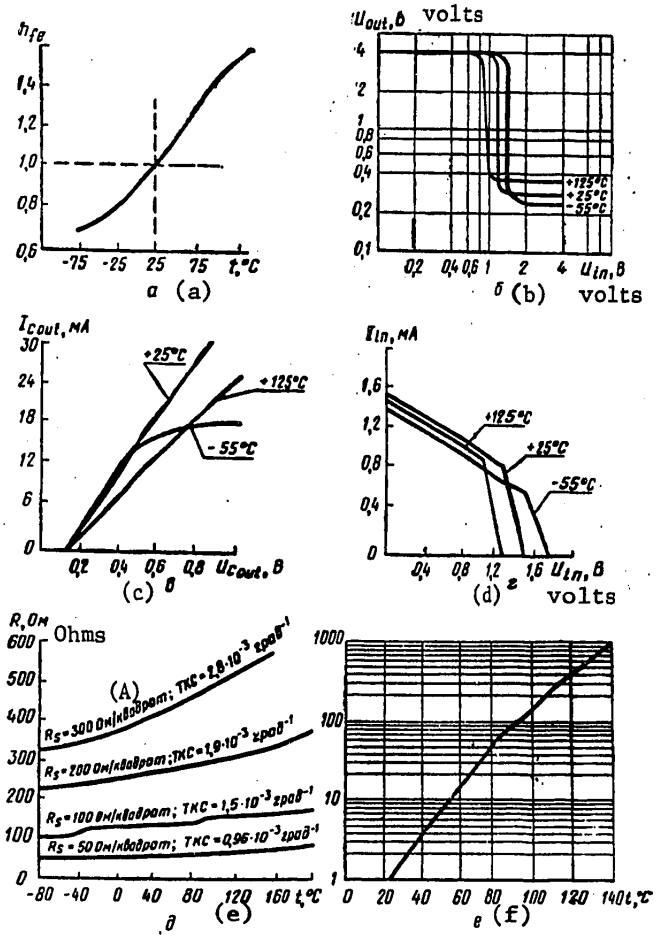

Figure 8. The temperature dependence of the current gain of a silicon transistor (a), the transfer function of a typical DTL circuit (b), the collector saturation voltage (c), the input characteristic of a typical DTL circuit (d), the resistance of a resistor (e), and the inverse current of a silicon p-n junction (f) is the theoretical curve.

Key: A. R_S = 300 ohms/square unit; temperature coefficient of resistance = $2.8 \cdot 10^{-3}$ deg^{-1}.

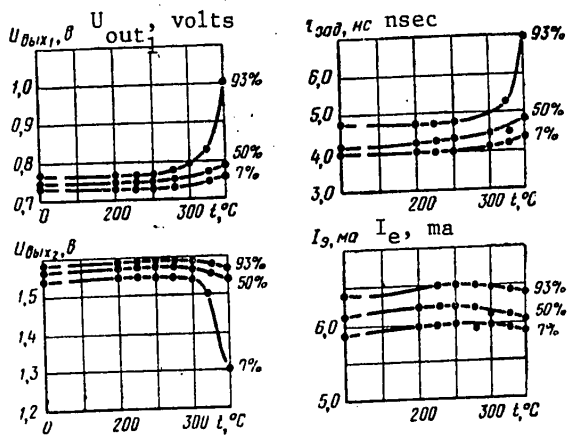

Figure 9. The major electrical parameters of a three-input "NOR" logic gate as a function of the ambient temperature.

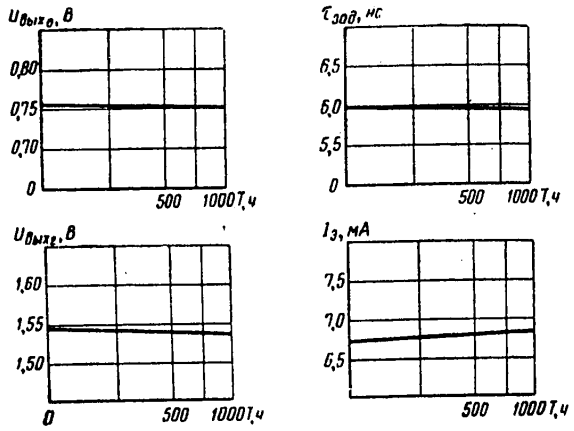

Figure 10. The change in the main electrical parameters of a three-input "NOR" logic gate during reliability testing.

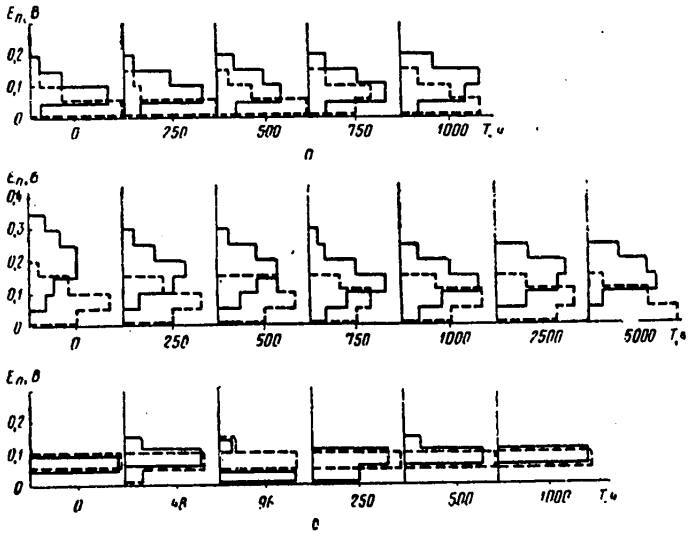

Figure 11. Histograms for the change in the voltage of three-input logic IC's during service life tests at +125° C (a) and storage life tests at +150° C (b) and +300° C (c).

Gradual failures comprise only an insignificant portion, thereby attesting to the high "inherent" (inherent in semiconductor IC's) reliability of these electronic products. The results of IC reliability tests at an ambient temperature of +125° C in a volume of about 13 million circuit-hours are given in [22]. Only in 0.68 percent of the IC's did the amount of parameter drift exceed the set norm. In the example cited in [4], the lack of any failures at all in IC's is indicated which were tested in an amount of 3, 626 units in an "ring oscillator" circuit at E_n = 3 volts and an ambient temperature of +125° C for 11, 845 hr.

The typical distribution of the parameters and the change in them during the testing process can be seen from Figure 11, in which the results of shelf-life and service life tests of MECL three-input IC's are shown. The high stability of the parameters is noted. At an ambient temperature of +300° C, the rate of drift in the main parameters did not exceed a value of 0.00001 [23].

As is well known, temperature cycles and shocks, humidity, a gas contaminated environment, mechanical loads, radiation and other factors have an impact on IC reliability during operation in addition to the factors considered here. Devices manufactured with high quality easily sustain all of these loads within the limits of the norms specified in the technical specifications, testing

programs and other standard setting engineering documentation. The IC failure distribution during climatic and mechanical tests shown in Table 6 clearly illustrate the assertion concerning the capability of IC's of successfully standing up to exposure to such loads [23]. As follows from Table 7, burned-in IC's stand up to more than 100 thermal shocks. A cyclical change in the ambient temperature has a negative influence on poorly mounted microcircuits, as well as on microcircuits in which materials with substantially different thermal coefficients of expansion are used. For example, the use of an unsuccessfully selected molding composition used to hermetically seal the IC's in plastic packages can cause the welded contacts to break or short circuits in the wire leads at the surface of the chip. The voltages which occur when the temperature changes and which are due to the differing thermal coefficients of expansion of the materials, is the reason for this. Thermal shock can accelerate the breaking of poorly made connections, etc. [4, 18, 27, 32].

Studies of the resistance of IC's to sea fog and tropical climate have made it possible to establish the fact that the packages of the devices limit the operational possibilities for IC's.

The mechanical strength of integrated semiconductor circuits exceeds the technical capabilities of the test equipment in the overwhelming majority of cases. The greatest number of IC failures during shock strength tests and tests for resistance to linear acceleration are observed at loads which are either never or extremely rarely encountered in operation. The most vulnerable section in IC's are the internal leads which connect the chip to the external leads. They usually break during centrifuging. However, this occurs at an acceleration many times greater than the level encountered in equipment operational practice. For this reason, by setting strict requirements on the level of the test load (up to 30,000 g), the requisite strength safety margin can be assured.

The radiation immunity of IC's falls at the level of the radiation resistance of silicon planar transistors and is limited by the latter.

According to [27-30, 32], modern semiconductor IC's stand up to operational loads in the following ranges: linear acceleration of from 50 to 50,000 g for standard products and up to 100,000 g for samples fabricated in accordance with special programs; in a temperature range of from -196 up to +200° C in the case of thermal shock; up to 280° C for soldering and up to 1,100° C in an inflammability test; from -185 to +300° C in a thermal cycling test; in terms of moisture immunity and moisture resistance at about 100 percent humidity, in a temperature range of 2 to 96° C; in terms of resistance and immunity to a salt fog, at 71° C and 20 %, in a salt solution, up to 10,000 g shock acceleration for a shock pulse width of from 0.2 msec to 6 msec; in terms of vibrational strength and vibration immunity at accelerations of from 5 to 2,000 Hz, and a displacement amplitude of no more than 2.5 cm and a vibrational acceleration of up to 100 g.

We will note in conclusion that the predominance of IC catastrophic failures, among which the greatest specific weight belongs to failures due to poor quality connections, makes it possible to suppose there is a real possibility of a

TABLE 6. Failure Distribution as a Function of the Kind and Magnitude of Test Load

Kind of Load	Test Conditions	Maximum Number of Failures, %
Thermal shock	0--100°C; 5 to 270 shocks	0.71
Thermal cycling	-60 + 175°C; 5 to 160 cycles	0.30
Tropical humidity	-10 + 60°C; 90 to 98 %; 1,200 hr	
	Period from 0--500 hr	0
	Period from 500--1,200 hr	1.40
Mechanical shock	3,000--10,000 g; 5 to 125 shocks	1.40
Vibration:		
At one frequency	60 Hz, 20--50 g; 96 hr	0
In a range of frequencies	5 to 500 Hz; 20--50 g; 1 hr	0.4
Constant acceleration	150--50,000 g; including 150--20,000 g	0
	above 20,000 g	1.3

TABLE 7. The Results of IC Tests for Exposure to Thermal Shocks

Number of Shocks / Количество ударов	(1) Пределы изменения температуры в рамках одного термоудара: от 0 до 100° С — выборка, шт. (2)	от 0 до 100° С — число отказов, шт. (3)	от −65 до +175° С — выборка, шт. (2)	от −65 до +175° С — число отказов, шт. (3)	от −200 до +200° С — выборка, шт. (2)	от −200 до +200° С — число отказов, шт. (3)
10	70	0	32	0	27	0
50	64	0	26	2	16	0
100	45	0	12	0	5	0
500	33	2				
1000	24	3				
1500	14	5				

Note: Exposure time is 30 minutes.

Key: 1. Range of temperature change within 1 thermal shock;
2. Sample, number of units;
3. Number of failures, units.

further increase in IC reliability in the immediate future. As was noted above, working out individual production process operations, refining the package protection, automating production processes, improving the metrological production support and refining the quality control system for the output product as a whole will assure the elimination of substantial sources of failures and the attaining of the reliability inherent in solid state components.

TABLE 8.

Виды испытаний Kinds of Tests	(1) Уровень надежности ($\lambda_{ср.}$, r^{-1})				
	10^{-5}	5.10^{-5}	10^{-6}	10^{-7}	5.10^{-6}
	(2) Максимальные затраты на одну микросхему, долл.				
	0	3	5	10	100
Электрические (функциональные) (3)					
Термоциклирование (4)					
Центрифугирование (5)					
Проверка герметичности (6)					
Электротермотренировка (7)					
Специальные испытания (8)					
Рентгенодефектоскопия (9)					
Квалификационные испытания (10)					
Испытание на долговечность (11)					
Климатические испытания (в полном объеме) (12)					
Проверка прочности сварных соединений (13)					

Key: 1. Reliability level (λ_{avg}, r^{-1}); 2. Maximum expenditures per IC, dollars;
3. Electrical (functional); 4. Thermal Cycling; 5. Centrifuging
6. Checking the hermetic seal; 7. Electrical & thermal conditioning;
8. Special tests; 9. X-ray flaw detection; 10. Qualification tests;
11. Operating life testing: 12. Climatic tests (in the full volume);
13. Checking the strength of the welded connections.

A consequenc of the substantial improvement in IC quality is a perceptible decrease in the number of complaints of substandard products, a reduction in the volume of periodic tests and tests of the nonfailure operating time as well as increased consumer confidence in the product manufacturer.

Reliability studies of domestic semiconductor IC's which have been conducted in recent years attest to the fact that the reliability which has been achieved comes up to the world state of the art and further efforts in this field should be made circumspectly, carefully weighing the economic expediency. The implementation of those measures to improve IC reliability and quality should be avoided which can be classified as superfluous and related to excess expenditures on quality control.

Quality improvement programs should be worked out on the basis of several reliability levels for the output product. Naturally, each of the levels should have its own corresponding cost expression. General and special technical specifications on IC's should provide for the possibility of the coordinated delivery of products to a consumer having permissible deviations from the specified requirements. Generalized data which illustrate these kinds of programs, which are widely used in the U.S. and other developed capitalist nations, are shown in Table 8.

Chapter III. The Main Kinds, Reasons for and Mechanisms of Semiconductor Integrated Circuit Failures

An analysis of the reasons for the failure of IC's during operation and testing makes it possible to establish the fact that at the present stage of microelectronics development, a characteristic feature is the predominance of failures, as a rule, due to the destruction of some of the structural components as a consequence of the imperfection of individual production process operations in IC fabrication and various violations of the standard setting engineering documentation in their application stage. This is clearly seen from Table 9, in which the generalized distributions according to kinds and causes of IC failures are presented [27, 28, 31-38]. Improving the structural design and fabrication technology of IC's will lead to a substantial increase in their reliability, which is evidenced by Figure 5, in which the averaged curve for the reduction in the failure rate of semiconductor integrated circuits over the period from 1961 through 1972 is shown based on generalized data (from various foreign sources) [27, 32, 33, 30, 39, 40]. The curve for the reduction in the failure rate after 1968 becomes flatter. This is explained, first of all, by the fast process of refinements in the structural design and working out the technology for bipolar IC's in the initial period of the introduction of this technology, and secondly, by the increase in the complexity of the technology and the rise in the level of integration, characteristic of the later developmental period of microelectronics [27].

A major source of total failures of IC's, as can be seen from Table 9, is the destruction of the electrical circuit. Reasons for breaks in the electrical circuits of IC's are inadequate strength of the welded connections, the occurrence of undesirable transition metal compounds in the contacts of materials of different kinds, as well as mechanical, electrical and chemical destruction of thin film metal conductors and assembly defects in the IC's.

The main causes of short circuits in the electrical circuits of IC's are defects in the photolithography and dielectric films, the occurrence of channels with the opposite type of conductivity, body defects in the crystal lattice of the semiconductor material as well as defects in the assembly of the IC's.

Gradual failures manifest primarily as an increase in the leakage currents and are caused by such factors as the appearance of channels with the opposite type of conductivity due to the migration of the mobile charge in the oxide film and the contamination of the surface of the semiconductor chip and the IC package. Where such defects are present, as well as in the case of a failure to seal by the package with the exposure to the ambient atmosphere, individual electrical parameters of an IC can gradually change their values ("drift"), something which in turn can lead to equipment failure.

We shall treat the physical and chemical processes which lead to IC failures.

Microcircuit failures encountered in practice are shown schematically in Figure 12; they can be conventionally broken down into three categories:

--Failures related to phenomena in the body of the semiconductor chip;

TABLE 9. Generalized Failure Distributions of Integrated Circuits According to Kinds and Causes of Failures

Kind of IC Failure	Cause of Integrated Circuit Failure	Number of Failures*, %		
		Average	Minimum	Maximum
1. Welded connection break	Poor mechanical strength of the weld connection (poor weld strength, poor adhesion of the contact area to the substrate). Mutual diffusion of the metals and the formation of transition metal compounds in the region of the weld. A reduction of the cross-section of a wire in a "heel". Exceeding the permissible levels of mechanical loads.	20	5	57
2. Breakage of thin film resistors and conductors	Mechanical damage, undercutting, unsatisfactory deposition of the relief steps, etc. Exceeding the permissible current level. Chemical and electrochemical corrosion. Unsatisfactory stripping of windows underneath contacts.	20	3	26
3. Increased leakage currents and short circuits	Contamination of the surface of the dielectric passivating films and the package. Dirt and defects in the dielectric films. Exceeding the permissible voltage level ("spikes", static electricity).	22	12	34
4. Failures due to photolithography defects	Parasitic ("false") diffusion due to photolithography defects. Inadequate etching and overetching oxides and metals. Incomplete removal of the photoresist.	10	5	24
5. Failures due to body defects in the crystal chip	"Punch-through" breakdown in transistors with a thin base. Breakdowns at the sites of local defects in the structure of the semiconductor crystal.	10	2	24
6. Failures due to defects in the package, in assembly and hermetic sealing	Poor hermetic seal of the package. Corrosion of the package components; mechanical damage and excessive tension on the flexible wire leads. Poor mechanical strength and high thermal resistance at the points of chip "seating" on the package base. Dirt and foreign particles in	15	2	31

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TABLE 9. [cont.]

Kind of IC Failure	Cause of Integrated Circuit Failure	Number of Failures*, % Average	Minimum	Maximum
	the package.			
7. Other	Damage to the package or labeling.	3	0	24

*With the exception of failures due to incorrect use of the IC's, which comprise from 5 to 72% of all failures.

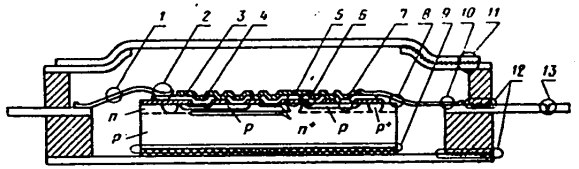

Figure 12. Critical points and typical kinds of failures of a planar epitaxial IC, fabricated using a single-level layout in a flat glass-metal package.

Key: 1. Breakage of the flexible conductor; 2. Breakage of the welded contact on the chip; 3. Leakage because of phenomena on the chip surface (including the Si--SiO_2 separation boundary); 4. Breakdown (punch-through) of the p-n junction (of a transistor); 5. Short circuit due to oxide film breakdown; 6. Breakage of a thin film conductor; 7. Breaking of the ohmic contact to the silicon; 8. Short circuit of a flexible conductor on the chip; 9. Increase in the thermal resistance or breakage of the contact of the chip to the package; 10. Breakage of the welded contact at the support piece; 11, 12. Loss of hermetic seal of the package in the region of the sealed seam (11) and the glass insulator (12); 13. Breakage of the external package lead.

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--Failures which depend on the state of contact connections;

--Failures due to phenomena at the surface of a chip.

1. Failures Related to Phenomena in the Body of a Semiconductor Chip

The appearance of failures related to body defects is explained either by the redistribution of the doping impurities in the body of the crystal chip or by structural defects in the semiconductor crystal (dislocations, stacking faults, microcracks, etc.), which occur or develop during the process of operating a defective IC.

The redistribution of impurities is theoretically possible because of the continuously ongoing thermal diffusion of doping impurities used to create the IC structure in a monocrystalline sample of a semiconductor material. However, there is little probability that this process plays a substantial role in practice, since the diffusion coefficients of the doping materials (boron, phosphorus, arsenic, antimony, etc.) in a silicon monocrystal are insignificantly small in that temperature range where IC's are used (from -60 to +125° C).

The most probable cause of failures related to phenomena in the body of a chip are defects in the semiconductor material. Dislocations and other defects of the crystalline structure, as well as cracks, deformations and mechanical stresses in a silicon crystal, developing during operation of the IC when exposed to thermal and mechanical loads, can have a substantial impact on changing the electrical characteristics of integrated circuits, leading primarily to gradual failures.

With an increase in the level of integration, which is characteristic of the state of the art in microelectronics, a trend is observed towards an increase in the "stacking density", a reduction in the geometric dimensions of active and passive IC components and a reduction in the doping depth of the p-n junctions related to this, as well as in increase in the level of doping of the diffusion regions of the semiconductor crystal and the electric field intensity in the IC elements.

Because of this, the degree of influence of local defects of the semiconductor structure on IC reliability increases. The major mechanisms for the degradation of the properties of epitaxial and diffusion layers of IC's with "small" p-n junctions are the motion of dislocations, a change in the internal stresses of the crystal lattice, recrystallization and breakdown of solid solutions, etc. [41-43]. The indicated processes lead to a change in such important characteristics as the concentration, mobility and lifetime of the current carriers in the semiconductor, and as a rule, to an increase in the leakage currents, a reduction in the breakdown voltage values for the junctions and a degradation of IC speed.

We shall now move on to a consideration of failures related to contact joints.

2. Failures which Depend on the State of Contact Bonds

Two types of contact connections are usually employed to connect an IC chip to external power supplies, as well as to provide for electrical connections between the circuit components. The first type is a connection of the thin film metal contact areas on the silicon chip to external leads which pass through the wall of the package (traverses). Such connections are made using gold or aluminum conductors, which are welded to contact areas of the chip and the package traverses. The second type of connection is thin film metal conductors, which play the part of the intracircuit wiring between the individual components on the IC chip.

When producing the contact connections in IC's, a considerable amount of different kinds of materials is used (gold, aluminum, silicon, cermet and silicide connections, sublayers of molybdenum, vanadium, platinum, titanium and other difficultly fusible metals, etc.), the interaction between which promotes the formation of transition metals, frequently with undesirable properties.

Failures related to contact connections, as a rule, take the form of an increase in the contact resistances or breaks in the electrical circuits due to two mechanisms:

--The clustering of vacancies in different regions of the wiring layout internal to the circuit;

--The formation of regions with electrical insulating properties, which occur at the separation boundaries of the various materials used in the construction of the IC's [31, 44-46].

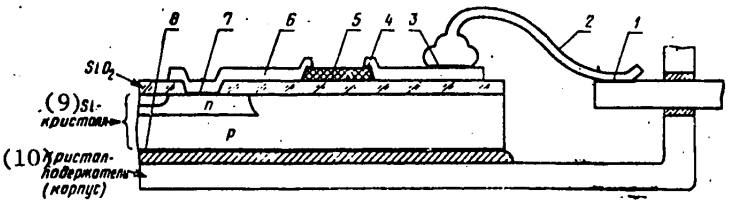

Figure 13. Regions of possible cavity formation in an IC with one level of metallization.

Key: 1. The metal to metal welded contact at the package feedthrough;
2. Flexible (wire, lug) lead;
3. Welded metal to metal contact at the chip;
4. Contact between the deposited resistor and a thin film metal conductor;
5. Thin film resistor;
6. Thin film metal conductor;
7. Metal to semiconductor ohmic contact;
8. Contact between the chip and the chip holder of the

package (fused, glued);
9. Si chip;
10. Chip holder (package).

A cross-section through the components of the internal wiring layout of IC's is shown schematically in Figure 13, where this layout is based on single level metallization and regions are indicated in which cavity formation and breaks are usually observed because of the clustering of vacancies (regions 1, 3, 4, 6, 7 and 8).

Welded Contacts. One of the most well studied regions of the intracircuit wiring of IC's in this regard is, apparently, the region of the welded metal to metal contact, in particular, the gold to aluminum connection.

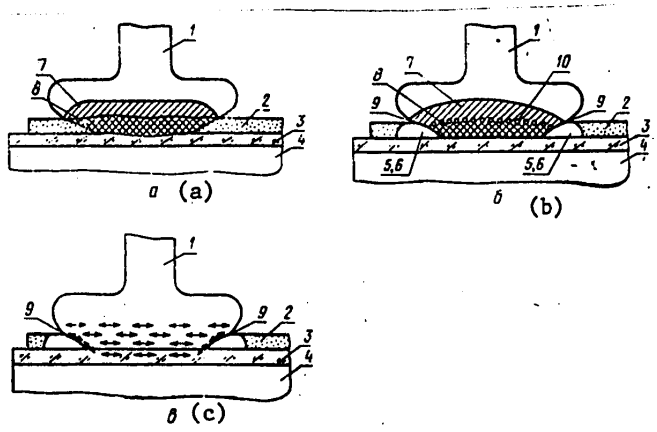

Figure 14. Cross-section through a Au--Al connection after 5 to 10 minutes exposure to a temperature of about 300° C (a) and after 10 to 1,000 hours of high temperature storage at a temperature of 200 to 300° C (b). Mechanical stresses in the welded joint which lead to contact breaking are shown schematically in the figure (c).

Key:
1. Au;
2. Al;
3. SiO_2;
4. Si;
5. Au_2Al;
6. $AuAl_2$;
7. Au_4Al;
8. Au_5Al_2;
9. Cracks;
10. Cavities.

The composition of transition metal compounds (phases) in gold to aluminum contacts is complicated and changes, depending on the conditions under which the composition is produced (the concentrations of gold and aluminum, the presence of free silicon, the temperature and pressure during the welding process, the ambient temperature and the operational time of the finished IC) as well as many other factors. The formation of transition metal compounds and the change in their composition during operation lead to cavity formation because of the accumulation of vacancies due to the Kirkendall effect, the occurrence of mechanical stresses at the surface of the gold--aluminum separation boundary, and in the final analysis, to breaks in the welded connections.

The mechanism for the failure of welded contacts produced by thermal compression is usually as follows [47-52]. During the process of thermal compression welding, which is accomplished at a substrate temperature of 300° C, the mutual diffusion of the gold and aluminum takes place, which leads to the formation of transition metal phases of the Au_2Al type at the gold--aluminum separation boundary (close to the gold wire) and $AuAl_2$ type (close to the aluminum contact area on the oxidized surface of the chip). In this case, because of local heating in the contact region, the temperature rises up to the minimal melting temperature of the gold--aluminum system, and the fusion occurs only in a small amount at the separation boundary of these metals.

During the fabrication of the remaining thermal compression contacts for the same IC, the substrate is at a temperature of about 300° C, which leads to rapid thermal diffusion of the gold and the formation of transition metal phases of the Au_4Al and Au_5Al_2 types in the region of gold--aluminum bonding (Figure 14a). Immediately following the welding, the contact connections usually have good mechanical and electrical properties. However, in the process of subsequent operation or when the IC is stored at an elevated temperature, irreversible phenomena occur which cause the electrical resistance to increase and the thermal compression contacts of the IC's to break. The concentration gradient of the metals and the difference in the diffusion coefficients of the individual components in this metallurgical system are those conditions under which a mass transport effect is observed (the Kirkendall effect) in accordance with the equation:

$$X = \sqrt{0{,}51 \cdot \exp\left(-\frac{23500}{RT}\right) t}, \qquad (1)$$

where X is the displacement of the separation boundary between the transition metal phases relative to its initial position, cm;
R is the universal gas constant;
T is the absolute temperature, °K;
t is the exposure time to the given temperature, °C.

It follows from this that failures related to the formation of transition metal phases in gold--aluminum contacts of IC's should be manifest extremely rarely under normal operating conditions. This conclusion is confirmed by extensive experimental data obtained during IC testing and operation. Nonetheless, since

the gold diffusion rate greatly exceeds the aluminum diffusion rate in the model described here for thermal compression contact degradation, with longterm operation of a finished IC at the maximum permissible temperatures according to the technical specifications, uncompensated diffusion of the gold into the aluminum track is altogether possible, in which case, the $AuAl_2$ transition metal phase with a red shading (the "purple plague") is formed at the peripheral areas of the gold--aluminum contact. In this case, cavities and cracks remain in the region of the weld which reduce the mechanical strength of the contacts (Figure 14b). The indicated process of gold diffusion into aluminum can be supplementally accelerated by the electromigration of the gold when DC or AC flows through the contact. Electromigration processes in integrated circuits will be treated below.

The formation of transition metal phases and the changing of their composition during operation of integrated circuits also leads to the occurrence of considerable mechanical stresses at the surface of the gold--aluminum separation boundary, because of the variation in the body and the mismatching of the crystalline lattice of the various transition metal compounds. The stresses occurring in this case can be amplified by the presence of additional mechanical stresses at the periphery of the thermal compression contact, as well as by the difference in the temperature coefficients of expansion of the individual transition metal phases (Figure 14c). All of these factors, in conjunction with the increased brittleness of many transition metal phases, can lead to breaks of the gold conductors away from the aluminum areas.

The proposed mechanism is confirmed in many respects by experimental results and has made it possible to provide a reasonable explanation for the given phenomenon.

However, the latest studies [44, 53-55] have necessitated corrections in this mechanism, since the newly obtained results could not, at first glance, be explained by the Kirkendall effect.

It was found, in the first place, that the clusters of vacancies which lead to the appearance of cavities, occur under definite conditions in aluminum, and this is evidence that aluminum is a faster diffusant. Secondly, it was established that the process of aluminum diffusion into the weld region is substantially accelerated in the absence of oxygen in the internal atmosphere of the IC package.

However, it was successfully determined as a result of additional experiments [44] that the observed phenomenon is also explained by the Kirkendall effect if one takes into account the fact that the transition metal compounds formed in the region of the weld act as a barrier for the mutual diffusion of the gold directly into the aluminum, while they also serve as an effective drain for both the gold and the aluminum. It is specifically for this reason that cavities (breaks) can be formed both in the gold and in the aluminum in welded Au-Al connections.

The influence of the gas environment in the IC package on the process of mutual diffusion in "gold--aluminum" contacts [54] is explained in the following manner. When oxygen and water vapors are absent (the hermetic sealing is carried out in

a dried nitrogen atmosphere) with subsequent high temperature storage, the predominant mechanism is the diffusion of the aluminum into the region of weld. In this case, the diffusion takes place primarily along the surface of the aluminum film and along the grain boundaries. In the case where oxygen is present inside the package in a minimal amount, but nonetheless sufficient (no less than 0.1%) (or water vapor also), when the IC is heated, oxidation of the aluminum surface occurs, and the rate of its diffusion is substantially retarded, since under these conditions, the predominant mechanism is bulk diffusion.

Aluminum wire is used in place of gold to completely eliminate failures related to the formation of transition metal compounds at Au--Al contacts on a chip. However, conditions appear in this case for the phase transformation of Au_xAl_y on the gold traverse.

An additional factor which has a negative impact on the mechanical strength of welded connections is mechanical damage and undercutting etching of the contact areas during photolithography, during the checking of the functioning of the IC's on the plates, and the welding, which lead to a reduction in the contact surface area and should be rejected in a timely manner during IC fabrication.

For integrated circuits, especially the early designs which were hermetically sealed in plastic packages, the specific kinds of failures related to the welded connections are intermittent breaks and short circuits of the wire leads at the edge of the IC chip [27, 30, 56, 57]. The intermittent nature of the failures is explained by displacements of the wire leads relative to the chip due to mechanical stresses occurring in the IC structure when subjected to temperature exposures because of the difference in the temperature coefficients of expansion of the materials employed.

Many other kinds of contact connections are also used in IC's besides welded ones.

Vacuum Deposited Resistors. The most vulnerable component of integrated circuits fabricated using a combined technology is the thin film deposited resistor. Compositions which take the form of a mixture of two or more metal and ceramic components, for example, a mixture chromium and silicon monoxide, Cr-SiO, or the silicides $CrSi_2$, $MoSi_2$, etc., as was noted above, are usually employed as the material for a resistive film. The electrical connection of deposited resistors to other IC components is made by means of metallic thin film conductors (Al), where aluminum, as a rule, is deposited on a layer of a chemically neutral metal, which separates the metal and resistive films. This is done for the purpose of preventing a possible chemical reaction between the individual components of the resulting system. In the case of damage or too small a thickness of the separating film, a reaction between the aluminum and the material of the deposited resistor can lead to the formation of a transition metal compound, having dielectric properties, and as a result, can be responsible for a break in the electrical circuit in the region of the metal to cermet contact [87].

Electrolytic corrosion is of the greatest danger to integrated circuits with deposited resistors, the chips of which do not have additional protection with

dielectric films, to prevent the intrusion of moisture and ionic contaminants to the surface of the resistors [64, 31].

The corrosion of a resistive film takes place in several stages in accordance with the following scheme: the electrolyte initially interacts with the metallization at the positive contact (the anode), and then the products of this reaction interact with the cermet, leading to the formation of an electrically insulating film at the point of contact:

$$\left.\begin{aligned} &6Al + 6H_2O \rightarrow 6Al(OH)_3 + 3H_2\uparrow; \\ &6Al(OH)_3 \equiv 6H_3AlO_3 \rightleftarrows 6H^+ + 6AlO_2^- + 6H_2O; \\ &2Cr + 6AlO_2^- + 6H^+ \rightarrow 2Cr(AlO_2)_3 + 3H_2\uparrow. \end{aligned}\right\} \quad (2)$$

In properly designed integrated circuits (the chips protected with a SiO_2 film, hermetically sealed packages), the occurrence of failures because of this factor is practically eliminated.

Thin film metal conductors ("tracks") which provide for electrical contacts between the individual active and passive components of IC's through contact openings in the oxide film and which are produced in the corresponding regions of the chip by means of photolithography, are usually employed as the intercomponent wiring for integrated circuits. To obtain the indicated contact connections, as a rule, the method of aluminum deposition on the surface of an oxidized silicon substrate is employed with subsequent photolithographic generation of the "pattern" of intracircuit wiring and the melting of the aluminum to increase its adhesion (bonding) to the substrate material and improve the characteristics of the ohmic contacts to the silicon.

We shall deal with the kinds and mechanisms of failures of the ohmic metal to semiconductor contacts.

Metal to Semiconductor Ohmic Bonds. The metal to semiconductor ohmic contacts used for making electrical connections to the active and passive components of a semiconductor structure on a chip are one of the important components of contact connections of IC's which have an impact on their reliability. Requirements are placed on them as regards the ohmic nature of the contact and low electrical resistance, as well as the stability of the properties and the absence of processes which lead to the degradation of the properties lying below the diffusion regions and the p-n junctions [48, 53, 58-61].

The latter is especially important from the viewpoint of assuring reliability of structures with small junctions and with "full" emitters.

Some three failure mechanisms are basically characteristic of the ohmic contacts of integrated circuits [48, 53, 58, 60, 61]:

--The formation of short circuits in the region of etching holes or the appearance of "nodules", which lead to pinholes in the protective dielectric film above the contact windows to the silicon, because of electromigration processes in the IC conductors (the danger of failures because of this mechanism rises sub-

stantially for IC's with small p-n junctions and multilevel metallization); the formation of films with electrical insulating properties at the metal--semiconductor separation boundary, which lead to an increase in the contact resistances or complete electrical breaks in the ohmic contacts;

--Thermal diffusion of the aluminum into the silicon and short circuits at elevated ambient temperatures and with local overheating of the diffusion regions on the chips.

Failures of ohmic contacts related to electromigration effects will be treated in more detail in the next section. We shall deal with failures due to the formation of electrical insulating films and the thermal diffusion of aluminum into silicon, which are observed during operation or storage of integrated circuits at an elevated temperature.

The probability of breaks is increased where photolithography defects are present (insufficient opening of the windows) and in the case of an inadequate temperature when fusing in the ohmic contacts [48]. It should be noted that an excessively high fusing temperature can also lead to a break in the aluminum film at the oxide steps at the boundaries of contact windows.

In structures with a "full" emitter, which have found widespread application in integrated circuits with an increased level of integration [VLSI], the interaction reaction of aluminum with silicon dioxide represents a particular danger, which takes place rapidly at temperatures above 500° C [48, 53]:

$$4Al + 3SiO_2 \rightarrow 2Al_2O_3 + 3Si \qquad (3)$$

In this case, the SiO_2 is reduced to silicon, and the aluminum at the boundaries of the contact window for the "full" emitter approaches an impermissibly close distance, x, to the emitter junction (Figure 15), which can lead to a junction short circuit.

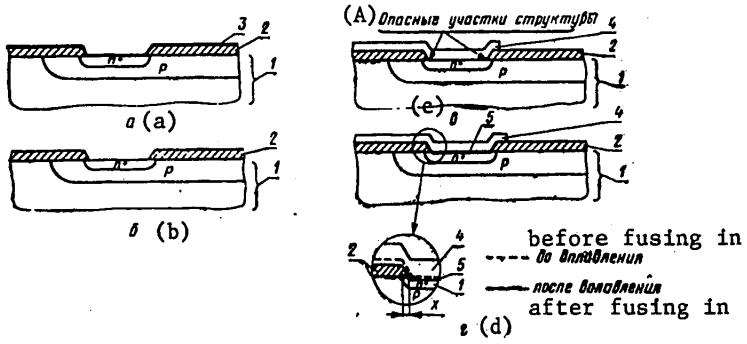

Figure 15. Schematic cross-section through a "full" emitter at various stages in producing the IC structure.
Key: A. Dangerous regions of the structure.

To prevent this undesirable phenomenon in integrated circuits with "full" emitters, multilayer films with sublayers of difficultly fusible metals (for example, Mo-Au, Mo-Al, Ti-Pt-Au, etc.) are used instead of "pure" aluminum when producing the thin film wiring layout.

Thin Film Interconnection Wiring. The increase in the level of integration of integrated circuits, and as a consequence, the packaging density of the components on a semiconductor chip, the increase in the speed and maximum frequency of integrated circuits, as well as the density of the currents flowing in thin film conductors have brought about an increase in the role of the intracircuit wiring layout and its contribution to IC reliability [31, 48, 58, 59, 62, 63].

Aluminum is used as the basic material for thin film conductors in integrated circuits. From a reliability standpoint, the major drawbacks of aluminum as a material for conductors are its following properties [48, 59]:

--The ability of aluminum to form large transition metal compounds in contact with gold;

--The ability of aluminum to corrode in electrolytes because of its own electronegativity [64-67];

--The possibility of the corrosion of aluminum in contact with other metals because of the galvanic effect [57, 68, 66, 69];

--The softness of aluminum and consequently, the ease of damaging an aluminum film;

--The possibility of the appearance of cavities and projections on an aluminum film because of electromigration at current densities somewhat less than for other metals [31, 34, 44-46, 58, 59, 70];

--The possibility of liberating silicon dissolved in aluminum during the process of fusing in the contacts at the boundaries of aluminum grains [44,46, 59];

--The rather intense reaction of aluminum with SiO_2 with the reduction of the silicon at temperatures on the order of 500° C [44, 53, 59].

Despite the indicated drawbacks, aluminum has a whole series of substantial advantages over other metals, which make it practically the only material suitable for producing single layer metallization of IC's, and for this reason, is widely used in modern microcircuit engineering [48, 58, 59].

One of the reasons for the failures of thin film conductors is the inadequate corrosion immunity of aluminum. The intrusion of moisture inside a package prior to its hermetic sealing or as a consequence of an inadequate hermetic seal of the package during the testing (or operating) process of an IC can lead to the destruction of the metallization. Only a thin film of Al_2O_3 (2 to 10 nm) on the aluminum surface serves to protect it against the chemical reaction of aluminum with water. However, a rather small amount of chlorine, ammonia or copper ions or those of certain other elements suffice for the passivating film of aluminum oxide to be reduced and the direct interaction of aluminum and water to begin,

in which aluminum hydroxide is formed [65]:

$$2Al + 6H_2O \rightarrow 2Al(OH)_3 + 3H_2\uparrow. \quad (4)$$

Aluminum hydroxide does not protect aluminum against exposure to harmful reagents and possesses electrical insulating properties. As a result, breakage of the electrical circuits of the IC's occurs.

Other aluminum reactions are also known in which the substances indicated above play the part of catalysts [67], for example, the following cyclical reaction:

$$\left.\begin{aligned} &6HCl + 2Al \rightarrow 2AlCl_3 + 3H_2\uparrow \\ &AlCl_3 + 3H_2O \rightarrow Al(OH)_3 + 3HCl \\ &2Al(OH)_3 \xrightarrow[\text{ageing}]{\text{старение}} Al_2O_3 + 3H_2O. \end{aligned}\right\} \quad (5)$$

which leads to the oxidation of the aluminum. The process of aluminum corrosion is accelerated substantially by electrochemical reactions:

--Where a voltaic couple of metals is present (for example, in the region of the gold--aluminum welded contact, a voltaic couple with a 3 V e.m.f. appears);

--When an external electrical bias is applied to the IC [28, 57, 64, 66, 68].

Anode dissolution of the aluminum at the "positive" contact is observed in these cases.

The processes of electrolytic corrosion of thin film conductors represent yet another danger, since disintegration products are formed during corrosion and electrical transfer of metal ions (for example, gold, silver) to the cathode is observed, which can lead to the appearance of shunting leaks and even to short circuits because of the formation of current conducting "bridges" between adjacent tracks [57, 65, 69]. The failure mechanisms described schematically above, related to the corrosion of the material of thin film conductors, are shown in Figure 16. Dielectrics (SiO_2, Al_2O_3 glass, etc.) are used to attenuate the effect of the indicated processes in integrated circuits. However, since windows should be formed in this insulating layer in the contact areas underneath the welded contacts, there exists the problem of circuit breakage because of metallization corrosion in the indicated regions.

Protecting the entire assembly with glass after laying out the leads unfortunately also cannot completely solve the corrosion problem, because mechanical stresses and cracks, which are formed in the glass during the process of assembly and hermetic sealing and with subsequent temperature loads on the IC, lead to local exposed places on the wire (lug, tab) conductors [57, 65, 66].

Electromigration (electrodiffusion) processes represent a definite danger for thin film conductors in IC's: mass transport as a result of the flow of an increased density direct current through a conductor [27, 31, 34, 45, 46, 59, 60, 70, 71].

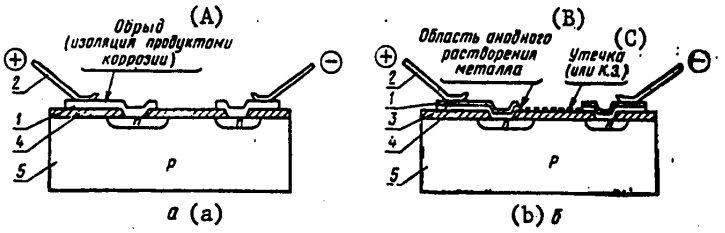

Figure 16. Schematic illustrating the mechanism of the occurrence of an electrical break (a) and a shunting leak (b) in IC circuits as a consequence of corrosion of the material of thin film semiconductors.

Key: 1. Al;
2. Au;
3. Mo;
4. SiO_2;
5. Si;
A. Break (insulation by corrosion products);
B. Region of anode dissolution of the metal;
C. Leak (or short circuit).

Electromigration in thin film aluminum conductors can lead to two different kinds of failures:

--The violation of the electrical integrity of aluminum conductors as a result of the formation, directional motion and clustering of vacancies, which leads to the formation of cavities commensurate with width of the thin film conductor (circuit breaks);

--The formation of "nodules" and "whiskers" because of a local accumulation of aluminum which is manifest in the form of short circuits between the thin film conductors of single and multiple level metalization and in the appearance of pinholes in the protective SiO_2 and glass films, which can subsequently serve as a cause of corrosion.

The electrical force acting on metal ions when an electrical current flows is composed of two components:

--The force of the interaction of an ionized metal atom with the electrical field (it is proportional to the electrical field intensity and the valence of the metal, and is directed towards the negative electrode) and the force of the "electron wind", which is governed by the impulse exchange between the charge carriers and the metal atoms (it is proportional to the specific resistance of the film and the current density, and is directed towards the positive electrode).

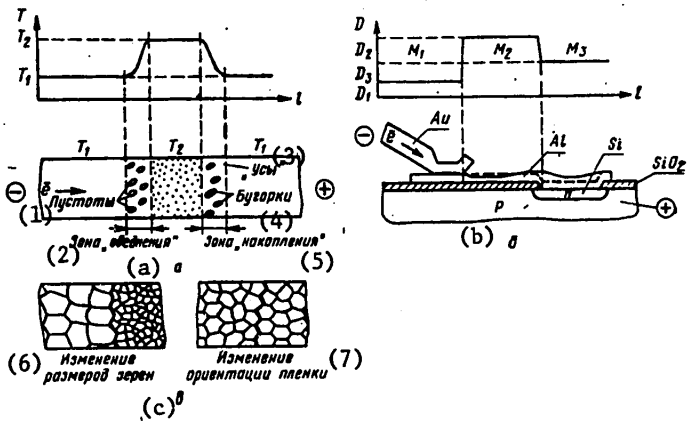

Figure 17. Schematic illustrating the mechanism for the occurrence of IC structural component failures because of electro= migration.

Key: 1. Cavities;
2. Depletion zone;
3. Whiskers;
4. Nodules;
5. Accumulation zone;
6. Change in grain size;
7. Change in film orientation.

The second component prevails in metals because of the shielding effect of the electrons, and as a result, the drift of metal ions is observed from the cathode to the anode.

In the absence of a temperature gradient, electromigration is not able in and of itself to bring about the failure of a conductor made of a pure homogeneous material, leading only to the continuous compensated motion of the metal in the direction of electron travel (towards the anode). In order for a break to occur in a conductor as a result of the electrical current flowing through it, the continuity of the flow of atoms over its length must be disrupted. This can occur where various gradients are present:

--Temperature gradients (Figure 17a);

--Gradients in the material composition (contacts of thin film conductors to gold, silicon and aluminum wire, which have smaller diffusion coefficients than an aluminum film) (Figure 17b);

--Film structure gradients: a change in the size and orientation of the grains (Figure 17c).

Electromigration in thin film conductors is usually estimated quantitatively in terms of the failure free operating time. The value of the mean time before failure, t_μ, of a thin film metal conductor is related to the transport speed for the material, R, and the cross-sectional area of the conductor, S, by the expression:

$$t_\mu = C \cdot \frac{S}{R}. \tag{6}$$

It is apparent that such defects in conductors as mechanical damage, undercutting of the film and local thin places lead to a reduction in the cross-sectional area of thin film conductors because of the unsatisfactory coverage of the steps with oxide and a reduction in their reliability because of the rapid development of the cavities which are formed prior to the stage of complete breakage.

The electromigration rate is described by the following expression [34, 46, 59, 60, 71, 72]:

$$R = A \cdot J^n \cdot \exp\left[-\left(\frac{\Phi}{kT} + \frac{\alpha}{L}\right)\right], \tag{7}$$

where A and α are coefficients which depend on the structure of the metallic film (grain size, the presence of additional protective films, the density of structural defects, etc.), $(A/cm^2)^{-n} \cdot hr^{-1}$ and centimeters;

J is the electrical current density through the conductor, A/cm^2;

n is the exponent which depends on the electromigration mechanism;

Φ is the activation energy for the electromigration process, which depend substantially on the composition of the film material, grain size and structural perfection of the metal films, as well as on the presence of protective dielectric films on their surface, electron-volts;

L is the length of the thin film conductor, centimeters;

k is Boltzmann's constant ($k = 8.62 \cdot 10^{-5}$ eV/°K);

T is the absolute temperature, in °K.

The exponential dependence of the electromigration rate on conductor length, L, was derived in [72] assuming a random nature for the localization and a constant distribution density of structural defects over the length of the thin film conductor.

It should be noted that different researchers obtain considerably different quantitative values for the "parameters" (A, n, Φ) in equation (7). These differences, as was noted above, are apparently explained by the substantial differences in the aluminum films themselves (grain size, crystallographic orientation of the

film, the presence of impurities in the material of the thin film (copper, silicon, aluminum oxide, etc.), unavoidable changes in the conditions on the substrate, the difference in the materials and methods of applying the dielectric coatings, the range of temperature and currents with which the experiments were performed and an entire series of other factors. Thus, for example, with an increase in the temperature of the conductor, the value of the exponent n varies from 1 to 3 [45] and more (especially in the case of the combined action of various gradients in the same conductor).

For the reasons noted previously, fundamental divergences are also observed in the treatment of the experimental results [45, 62]. Thus, the majority of researchers [46, 71-73] feels that the grain size and the coating of the films with glass has an influence on the activation energy Φ because of the change in the predominant diffusion mechanism:

--0.48 eV because of the combined action of diffusion via grain boundaries and surface diffusion in fine grained thin films;

--0.84 eV because of surface diffusion in large grained films;

--1.2 eV in large grained thick films, covered with glass, because of the dominant mechanism of bulk diffusion (with a reduction in the role of surface diffusion of the film material).

Other researchers assert that the grain size has no influence at all on the level of the activation energy [87] or feel that the increase in the activation energy observed in this case is a consequence only of a more ordered orientation of large grained films [45, 73].

All of this is evidence of the inadequate extent to which the process of electromigration has been studied and the necessity of determining the quantity A, n and Φ in equation (7) for specific conditions of the formation of thin film conductors and the application of dielectric films which coat metal tracks.

Despite such substantial disparaties in the quantitative characteristics of the processes, the understanding of the basic laws governing the mechanism of electromigration occurring in thin film conductors is useful both in the development of more reliable IC's and for the accelerated evaluation of their reliability (especially the durability indicators).

Short circuits of the p-n junctions due to the formation of etching holes in the silicon in the region of the contact windows represent yet another variant of failures related to electromigration in the thin film wiring layout for IC's [46, 60, 61]. This phenomenon is explained by the transport of silicon in the direction of electron travel through a thin film conductor (in the region of positively biased ohmic contacts) and the subsequent filling of the etching holes, which propagate at the depth of the p-n junction, with a layer of metal.

The electromigration process represents a special danger in very large scale integrated circuits [63, 71], since the substantial reduction in the width of thin

film conductors, the presence of a large number of relief steps at intersections, the rise in the current density at critical points and the occurrence of local overheating because of the increased levels of power dissipation - all of this leads to the fact that the electromigration process which occurs in the thin film conductors of LSI circuits can become the major mechanism for failures which governs the durability of the IC's.

Numerous studies of the electromigration mechanism in IC thin film conductors make it possible to determine ways of minimizing this process both in the design stages and in the process of fabricating the IC's [27, 31, 32, 45, 58, 59, 71]. These include primarily:

--Limiting the maximum permissible current density through an aluminium conductor to a value of $2 \cdot 10^5$ A/cm^2;

--Optimizing the conditions for applying and fusing-in the aluminum for the purpose of assuring a large grained structure for the thin film conductors;

--Optimizing the geometric dimensions and configuration of thin film conductors (if there are no other limitations, it is more expedient to increase the width of the conductors rather than the thickness in increasing the cross-sectional area, since this does not degrade the quality of the application of insulating and passivating SiO_2 films in a multilevel layout or the structure of the metal film itself; long conductors are to be avoided, as well as sharp changes in the width of conductors, etc.);

--The selection of difficultly fusible metals with a low electromigration rate for the thin film conductors (for example, gold, molybdenum, etc.);

--Alloying the aluminum with copper, magnesium, chromium and other metals which reduce its electromigration rate, as well as with silicon, for the purpose of preventing the appearance of etching holes in the contact windows with the semiconductor structure when electrical current flows through it;

--Applying protective dielectric coatings of SiO_2, Al_2O_3, etc. to the surface of the thin metal films, which make it difficult for "nodules" to grow (and consequently also cavities) in the conducting films;

--Monitoring the thickness of thin metal films (especially the degree of coverage of relief steps) using a scanning electron microscope;

--Visually monitoring the quality of the thin film wiring layout under a microscope for the purpose of rejecting IC's with defective current conducting tracks.

Multilevel Interconnection Layout. Because of the increase in the component placement density on chips in the production of very large scale integrated circuits, there has been a great growth in the role of multilevel metallization at the present time [28, 59, 62, 71, 74, 75]. When a transition is made to LSI circuits, as practice has shown, the prevalent types of failures become those related to the multilevel metallization [27, 63].

We shall consider problems of reliability related to the occurrence of new failure mechanisms which are characteristic of multilevel metallization, a schematic cross-section of which is shown in Figure 18.

There are three specific kinds of failures inherent in this structural component of IC's [62, 74, 75]:

--Disruption of the electrical contacts between the thin film conductors of the different levels;

--Short circuits between the thin film conductors of the different levels because of the presence of defects in the interlevel insulation;

--Breaks in the thin film conductors of the upper levels at relief steps in the lower metallization levels.

Strictly speaking, the latter type of failures is also observed in IC's with a single level of metallization, but with the transition to structures with multiple level metallization, its role increases significantly.

Contacts between the tracks of the different levels should have a low electrical contact resistance and a high current carrying capacity.

Failures of the first kind occur because of contact window opening defects in the interlevel insulation. Undercutting etching and complete overetching of lower level thin film conductors are observed, since the aluminum used at the present time as the basic material for thin film IC conductors actively interacts with a broad range of the etchants which are used. Moreover, it is difficult to assure a high quality coating of the lower layer of metal when depositing the upper metallization level in these regions because of the "shading" of the lower surface (bottom) of the contact window by its walls [75]. The electrical contact can be preserved in this case, however, increased resistance in this region can lead to IC failure during its operation.

Failures of the second kind are due to defects in the oxide film used as the interlevel insulation. Usually, the oxide layer is obtained by precipitation from the gas phase and is extremely inhomogeneous, in which case, the material of the lower layer as well as the geometry and thickness of the oxide can have an influence on its profile [62, 74]. If the edges of the thin film conductors are not smoothed off in this case, then microholes can be formed at the steep steps in the metallization, where these holes are potential sources of short circuits (see region 9 in Figure 18). Insufficiently careful cleaning of the surface prior to the application of the oxide, as well as unsatifactory monitoring of the composition and thickness of the deposited oxide film exacerbate this phenomenon. Effective techniques for solving this problem are smoothing off the edges of the thin film conductors and providing for an optimal ratio of the thickness of the metal layers and the oxide covering it (increasing the oxide thickness).

Shorts between the conductors of the different levels can also appear because of the growth of nodules ("little bumps") on the surface of the metal film during subsequent heat treatment [74].

The height of such bumps can reach a few microns, and the passivating layers of oxide or photoresist film cannot cover them, something which leads to undercut etching of the oxide and the metal. As a result, shorts appear between the conductors of the various levels when subsequent metallization levels are applied or during operation of the IC's with temperature and electrical loads.

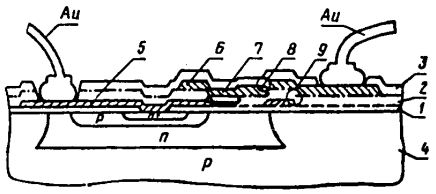

Figure 18. Cross-section through the structure of an integrated circuit made with two-level metallization (levels I and II) with a passivating protective glass surface.

Key:
1. "Thermal" SiO_2;
2. Precipitated SiO_2;
3. Passivating glass;
4. Si;
5. Lower metallization level;
6. Upper metallization level;
7. Contact between the conductors of the different levels;
8. Thinning of the upper level conductor at a relief step in the lower level;
9. Insulated crossing of the conductors of the different levels.

An effective means of preventing the formation of nodules and cracks in the oxide film is the use of a low temperature (< 400° C) passivating coating of SiO_2 of sufficient thickness (up to 100 nm). It is also recommended [75] that a combination of two technological processes be used for the application of the SiO_2 films (RF vaporization coating at a temperature of about 100° C with subsequent chemical precipitation of SiO_2 from the gaseous phase). In this case, the bottom (main) SiO_2 layer provides for good insulation, while the upper layer covers possible holes and smoothes the surface of the oxide film.

The third type of failure is breaks in the thin film conductors of the upper levels at steps in the lower levels and is the most probable kind, where rather high and steep relief steps are formed on which it is very difficult to apply a layer of metal in the process of producing the third and subsequent levels of metallization (Figure 19). The most effective means of eliminating this cause of failures is the technique of "smoothing off" the edges of the thin film conductors when producing the bottom (first) metallization level. However, it must be noted that the cross-sectional area of the thin-film conductors of the first level is approxi-

mately cut in half in this case (as compared to the initial value), which can lead to failures due to electromigration, if the reduction in the cross-section is not compensated beforehand [74].

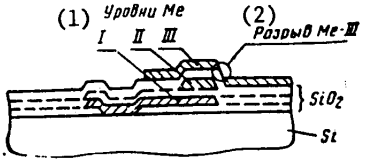

Figure 19. Break in a third level thin film conductor at the matching boundaries of conductors of metallization levels I and II.

Key: 1. Metallization levels;
2. Break in level 3.

Scientific research and design work are constantly under way to seek out new combinations of metals to produce reliable current carrying conductors and materials as well as a more refined technology for applying insulating films in structures with multilevel metallization so as to more fully utilize all of the advantages of multilevel metallization.

The most promising trends in this case are:

--Replacing aluminum as the main material of the conductors with multilayer thin metal films based on difficultly fusible metals [59, 58, 76];

--Using aluminum dioxide for the interlevel insulation of the films, where this oxide is obtained by means of anodizing, or using polyimide films [77, 78].

Thin multilayer metal films (Ti-Pd-Au, No-Au-No, Ta-Au-Ta, etc.) make it possible to:

--Increase the mean time before failure by one to two orders of magnitude (under similar operational conditions);

--Reduce the geometric dimensions of the current carrying conductors as compared to single layer ones with the same current density levels;

--Assure high adhesion and substantially reduce the probability of undesirable chemical interactions of metal films with silicon dioxide, silicon, moisture and surface contaminants of the chip;

--Markedly reduce the mutual diffusion rate of the metals (the Au-Au welded contacts).

All of these advantages completely justify increased complexity of the metallization system, especially for very large scale integrated circuits.

The use of new insulating materials as the interlevel insulation instead of traditional silicon dioxide makes it possible to:

--Substantially reduce the probability of failures due to short circuits between the conductors of the various levels as a consequence of the better electrical insulating properties and the smaller number of defects in the "barrier" Al_3O_3 oxide films and the polyimide films (as compared to SiO_2);

--Reduce to a minimum (in structures with Al_2O_3 dielectric insulation) or completely eliminate (in structures with polyimide insulating films) relief steps, which makes it possible to eliminate local thinning of the thin film conductors at relief steps of the lower levels of the wiring layout and to realize three to five level metallization for very large scale integrated circuits while preserving acceptable indicators for their reliability;

--Increase the resistance of multilevel metallization to thermal shocks because of the high elasticity of the polyimide.

In conclusion, we shall consider yet another kind of contact connection used in integrated circuits.

The Chip to Chip Holder Contact. In the process of mounting the chip in a package, it is fastened ("seated") in the chip holder by means of brazing using a gold-silicon eutectic or by gluing with a heat resistant glue (compound). It should be noted that "seating" the chip on a eutectic is more to be preferred because of the better mechanical properties and lower thermal resistance as compared to glued contacts.

As a result of contamination of the chip surfaces and the chip holder, or inadequately worked out conditions for the "seating" operation, nonuniform wetting of the surfaces being joined together with the gold (or glue) is sometimes observed, misalignment of the chip and other defects occur which lead to a degradation in the characteristics of the contact connection.

Nonuniform brazing or gluing (in particular, because of nonuniform wetting of the surfaces) in the region of the chip--chip holder contact connection (region 8 in Figure 13) can lead to the fact the IC's will contain cavities underneath the chips, although they pass all of the electrical tests. This defect can manifest both in an overall increase in the thermal resistance of the IC, and in nonuniformity of the temperature field in the chip, something which is the most dangerous for high power and linear IC's. The mechanical strength of such a contact is naturally reduced. It is specifically IC's with such weakened contacts which are the most inclined towards failures because of the difference in the temperature coefficients of expansion of the materials employed. This effect is especially pronounced in the accumulation of mechanical fatigue damage due to variable mechanical stresses which occur in the structural components with long term exposure of the integrated circuit to temperature gradients: thermal shocks, thermal cycling, and a cyclical variation in the dissipated power.

In this case, it is specifically a degradation of the contact connections which is observed first of all, and which leads in the final analysis to a gradual failure of the IC, especially in the case where it is hermetically sealed in a plastic package.

We shall now move on to a discussion of third category: failures related to the state of the integrated circuit surface.

3. Failures Due to Phenomena on the Chip Surface

Gradual failures due to surface instability of IC's and the influence of the environment comprise an important category of IC failures, especially in the case of an increased level of IC integration. The difficulty of achieving the high level of purity needed to preclude undesirable surface effects, the reduction in the dimensions of the components and the spacings between them, which leads to an increased electrical field intensity in IC's, as well as the wide scale application of an increased level of integration of MOS transistors with a thin layer of oxide under the gates in integrated circuits - all of these factors make the study of the influence of the surface migration of ions on MOS and bipolar IC reliability an extremely urgent problem.

The application of dielectric films to the surface of a chip for the purpose of passivating it or to form interlevel insulation in the multilevel metallization of very large scale integrated circuits can have a substantial impact on IC reliability because of the change in the following characteristics of the Si--SiO_2 system [30, 31, 47, 62, 79-81]:

--The amount of the mobile and stationary charge in the oxide;

--The stability of the charge in the oxide when exposed to an electrical field under elevated temperature conditions;

--The surface recombination rate.

We shall consider the possible reasons for these failures. As is well known, when using planar technology, the electron--hole junctions are formed by the diffusion of doping impurities into the silicon through local openings in the silicon dioxide film which are produced photolithographically. In this case, the oxide layer serves as a masking coating, performing the functions of a "barrier" for the doping impurity (boron, phosphorus, etc.), which is necessary to produce the individual IC components in accordance with the specified topology.

After fabricating the device, the oxide film remains on the chip surface and protects the p-n junctions from the environment, thereby performing the functions of a passivating and stabilizing coating. However, charges of a diverse nature are present on the surface and within the oxide (the positive and negative ions of the doping impurities, excess ionized silicon atoms, electrons, holes, "traps", etc.), which are symbolically depicted in Figure 20 [82]. During integrated circuit operation, the redistribution of the electrical charges takes place at the Si--SiO_2 separation boundary and the near-surface region of the semiconductor crystal, where this redistribution causes significant changes in the characteristics of the p-n junctions and sometimes leads to the appearance of surface channels with an inverse silicon conductivity ("inverse" channels). Because of this phenomenon, the leakage currents rise and the IC parameters are substantially degraded [62, 79, 83].

The kinetics of the process which leads to the formation of inverse channels in integrated circuits is shown in simplified form in Figure 21 (a-c). The oxide layer which coats the chip of an actual IC takes the form of an amorphous

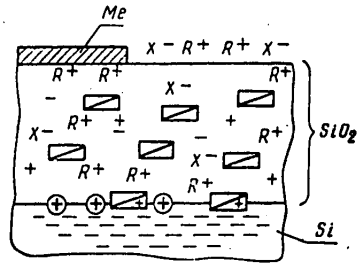

Рис. 20. Схема распределения зарядов, возникающих в окисной пленке:
R^+, x^- —ионы на поверхности и внутри
SiO_2; ⊕ Excess "ionized"
Si atoms; "traps"
-,+ Electrons and holes..

Figure 20. Schematic of the distribution of the charges occurring in an oxide film.
R^+ and x^- are ions at the surface and inside the SiO_2.

structure, the basis for which is silicon, phosphorus and boron atoms bound with oxygen atoms. Moreover, atoms of such alkali earth metals as sodium, potassium and lithim are usually present in the oxide. The concentration and mobility of these ions (and other contaminants) is especially high in the case of insufficiently effective cleaning of the surface of the plates prior to oxidation or contamination during the process of applying (growing) the oxide or where a high density of defects is present in the oxide film. The metal ions are positive, and in having a high mobility in the oxide structure, can easily move in the oxide layer to the Si--SiO_2 separation boundary when exposed to an electrical field. As a result of this, a bulk positive charge is formed in the thin oxide layer located directly at the separation boundary. The electrical field produced by the bulk charge of positive ions serves as the reason for the occurrence of local regions (channels) in the near surface layer of the silicon, which possess electron conductivity. The formation n-type channels causes the depletion or inversion of the conductivity of the p-type silicon and the accumulation of excess current carriers in the n-type material.

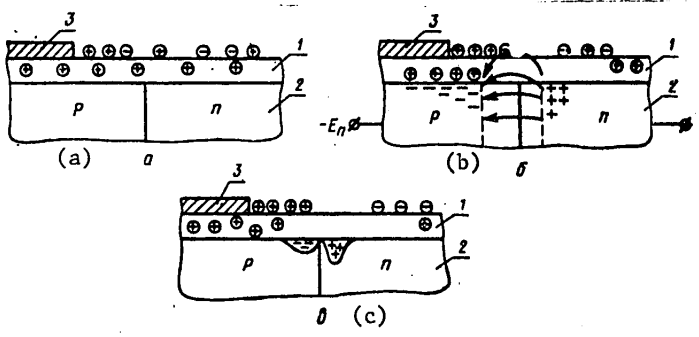

Figure 21. The sequential stages of charge separation by the electrical field in an oxide film and the formation of inverse channels on the surface of the silicon.

Key: 1. SiO_2;
2. Si;
3. Metal electrode.

It has been experimentally found that inverse channels can be eliminated by means of high temperature annealing without supplying inverse bias to the IC. However, the source of instability is not eliminated in this case and during subsequent IC operation at an elevated temperature, the channels are formed again.

MOS structures are the most sensitive to the state of the oxide, in which the effect of ion surface migration is substantially amplified by the overall impact of three factors:

--The oxide under the gate is the "working" element of the IC, governing its basic electrical characteristic: the threshold voltage;

--The thickness of the oxide under the gate usually does not exceed 150 to 200 nm, something which, first of all, makes it difficult to assure a perfect structure of the film, and secondly, leads to an increase in the electrical intensity in the critical region, and thirdly, reduces the spacing which the positive ions must overcome to reach the separation surface;

--The working supply voltages normally used to electrically drive MOS structures substantially exceed the voltages for the majority of logic planar epitaxial IC's [30].

The main kind of failures due to surface effects, characteristic of MOS IC's, is threshold voltage instability when they operate under conditions of elevated temperature and negative bias.

The design of integrated circuits of an increased level of integration with multilevel metallization, as well as with a single level of metallization coated with a layer of silicon dioxide (glass) exacerbates the problem of surface instability [47, 62, 81]. This is related to the fact that the additional protective oxides applied to the surface of the sufficiently perfect, thermally grown oxide, as a rule have a higher moisture content, degrading the properties of the silicon--silicon dioxide separation boundary.

Supplemental doping of the oxide with phosphorus (in the emitter diffusion state) is widely used to stabilize the surface, since the thin layer of phosphorus silicate glass (PSG) formed in this case has getter properties with respect to the alkali earth metal ions and plays the part of a barrier, actively impeding the accumulation of ions at the separation surface [47, 62, 79, 84].

It must also be noted that when applying a glass-like film of PSG to the surface of the oxide, its dielectric strength is increased at the same time, since the boundaries of the grains and microcrystallites, which reduce the breakdown voltage of the oxide, terminate at the PSG--SiO_2 separation boundary, not going out to the surface of the oxide.

However, care must be taken when alloying the oxide with the PSG layer, because the excessively high P_2O_5 concentration can lead to a shift in the threshold voltage because of the phenomenon of PSG polarization.

Such a type of failure as a short circuit of the thin film conductor at the silicon surface through holes in the oxide film are also to be numbered among failures

due to unsatisfactory surface states of IC chips. The reasons for this are usually various oxide defects (holes, punctures, microcracks, underetchings, etc.), which reduce its dielectric strength or which expose the surface of the silicon [47, 62]. In this case, only the small air gap between the metal and the silicon serves as the insulator, the dielectric strength in the local region falls off sharply (from $4 \cdot 10^7$ V/cm to $5 \cdot 10^5$ V/cm and less), and when a sufficient electrical voltage is fed to the IC, the conductor short circuits at the surface of the semiconductor chip.

One of the reasons for failures related to breakdown of defect free dielectric films, used in IC's with MOS structures, is the effect of static electricity discharges on the ultrathin (usually no thicker than 150 nm) dielectric films which insulate the gates. Thermally grown SiO_2 films or a combination of silicon dioxide layers with silicon nitride, $SiO_2 + Si_3N_4$, are used, as has already been noted, as the dielectric in MOS structures. Despite the fact that thin homogeneous films of the indicated dielectrics are immune to electrical fields of up to $4 \cdot 10^7$ V/cm, an irreversible dielectric breakdown can be observed in MOS structures at considerably lower intensities (about $4 \cdot 10^6$ V/cm), corresponding to a gate voltage of 50 to 80 volts [89, 90]. This is explained by the redistribution of the electrical field, where this redistribution generates local regions with an elevated field intensity in the near-surface region of the dielectric film at points where the gate metallization overlaps the peripheral regions of the p-n junctions (the drain and the source). Breakdown of defect free dielectric films in these regions occurs at voltages considerably less than the breakdown level for the p-n junctions of the MOS structure.

4. Other Kinds of Integrated Circuit Failures

Because of the high chemical reactivity of aluminum and a number of other metals used in IC's, as well as the extremely unfavorable impact of moisture and chemical contaminants on the properties of IC chip surfaces, the degree of hermetic sealing of IC packages is of particular importance from the viewpoint of reliability. The presence of microholes (leaks) in packages - defects in packages or the hermetic seal which are not detected in time or which appear during improper application of the IC's - which promote the penetration of water vapor, dirt, chemically reactive substances, etc. into the IC's during their operation, especially under conditions of elevated ambient humidity, can lead to failures due to corrosion of the thin film conductors and resistors as well as the occurrence of ion and inversion type leakage, the mechanisms for which were treated in detail above.

Unsealed soldered or welded seams and the points of metal to glass joints (especially in the case of incomplete fusion, incomplete wetting with solder, splitting and other mechanical damage to package components) are possible paths for the penetration of moisture, dirt, etc. into IC's. Moisture and contaminants can penetrate into plastic packages to the surface of the chips through pores in the plastic or along the surface of the separation between it and the metal leads (feed-throughs and flexible leads) [65, 66, 69].

An important cause of degradation which exerts a substantial influence on IC reliability is the corrosion of the metal parts of packages because of insufficient

thickness or mechanical damage to their anticorrosion coatings, as well as because of exposure of parts of the components fabricated from corrosion vulnerable metals, at points of cracking or chipping of the glass insulators.

Chemical or electrochemical corrosion of package components, primarily the external leads of a package, leads to IC failures in the external appearance or because of the tearing away (breaking) of the external leads during storage or operation of the IC with power applied under conditions of increased ambient humidity.

To eliminate the indicated reasons for failures, the most promising approach is the refinement of methods of checking the hermetic seal of IC's, which make it possible to ascertain leaks in the packages throughout the entire range of inflow rates.

During longterm operation or testing of IC's at an elevated temperature (on the order of 125° C), failures are observed in a number of cases which are related to the disruption of the electrical integrity of the soldered connections of the external leads of a microcircuit, with the leads made of gold plated Fernico, to the current carrying tracks on the printed circuit. The failure mechanism in this case is related to the dissolution of the gold in the lead-tin solder [91], which can lead to the occurrence of sections of exposed Fernico on the external leads of IC's (when they are mounted on a printed circuit board) and the subsequent degradation of the soldered contact quality (during subsequent operation of the IC's) in the case where the thickness of the gold coating of the external leads is insufficient, while the quality of the soldering of the IC to the circuit board is unsatisfactory ("point" soldering).

Such are the major kinds, reasons and mechanisms of the degradation processes which lead to failures of semiconductor integrated circuits.

In conclusion, we shall briefly treat the specific features of very large scale integrated circuits which influence their reliability and which are manifest in the redistribution of the dominant failures with respect to types and in changes in the kinetics of integrated circuit failures.

To define the trends in the change in the reliability of very large scale integrated circuits it is necessary to evaluate the impact of the following factors:

--Multilevel metallization with dielectric film insulation applied by precipitation techniques;

--The reduction in the dimensions of the active and passive components as well as the spacings between them;

--The increased power dissipation level per unit of chip area;

--The increase in the dimensions of the chip and package [32, 62, 71].

An analysis of the test and operational data existing at the present time large scale integrated circuits [27, 32, 33, 30, 62, 86] attests to the fact that with an increase in the number of gates on a chip, a redistribution of the types of failures takes place (see the comparative data in Table 10):

TABLE 10. Comparative Data on the Distribution of IC's with Respect to the Kinds of Failures as a Function of the Level of IC Integration

Reason for the Failure	Number of IC Failures, %: Low Level of Integration	Intermediate Level Integration	LSI: Bipolar	LSI: MOS Structure
1. Thin film conductors ("metallization")	16	25	27	4
2. Defects in the photolithography and diffusion	14	12	25	6
3. Defects in the structure and contamination of the oxide and semiconductor chip	26	25	14	54
4. Defects in the assembly and sealing (breaks in the welded contacts, defects in seating the chip, disruption of the hermetic seal, etc.)	28	12	6	-
5. Intrusion of foreign particles into the package	8	12	14	12
6. Other reasons for failures (including undetermined ones)	8	14	14	24
7. Incorrect use (in the form of the ratio of failures because of incorrect use to the total number of detected failures)	36	17	5	15

--For bipolar large scale integrated circuits (LSI), the specific percentage of failures related to the metallization, diffusion and intrusion of foreign particles into the package increases [27, 32];

--For LSI circuits based on MOS structures, the characteristic causes of failures are defects in the oxidation, charge instability related to contamination and defects in the photolithography [27, 31, 32, 33, 30, 62, 86].

Problems related to the use of multilevel metallization were treated in Chapter II. We shall now briefly touch on the influence of "dimensional effects" in large scale integrated circuits.

A substantial increase in the level of IC integration is manifest, first of all, in a sharp reduction in the geometric dimensions of individual elements (for integrated circuits of the third and fourth levels of integration, down to values on the order of 1 to 3 μm) and the spacings between them, and secondly, in the use of structures with "small" p-n junctions with submicron doping depths for the junctions and minimal thicknesses of the epitaxial layers, reaching 1 to 2 μm.

Obviously, elements with such small dimensions will be made with greater relative errors than the larger elements of integrated circuits of the first and second levels of integration, since the absolute errors in the fabrication of IC's given the technological state of the art will be approximately the same. In this case, considering the fact that concurrently with an increase in chip size, the number of defects occurring on its surface will also increase, the conclusion can be drawn that with a rise in the level of integration and when the present level of materials quality and technological process stability is maintained, the percentage of potentially unreliable IC's will increase. The reduction in the geometric dimensions of elements on a chip, besides increasing the criticalness of IC's to the layout precision and resolving power provided by photolithographic processes, the role of such failure mechanisms as corrosion and electromigration of the material of thin film conductors will increase markedly, as well as the formation of shunting leaks (shorts) between IC components, leaks and breakdowns of p-n junctions due to disruption of the diffusion profiles because of photolithography defects, etc. The influence of "small geometry" is manifest here in two ways: first of all, as was noted above, with a reduction in the spacings between the elements, there is an increase in the electrical field intensity between them, which increases the rate of degradation processes; secondly, the reduction in the width of thin film conductors, the doping depths of the p-n junctions as well as the spacings between the active and passive components and current conducting tracks on a chip increases the criticalness of IC's to the failure mechanisms indicated above.

All of this attests to the necessity of devoting special attention to questions of assuring the reliability of IC's with an increased level of integration in all of their production (design, fabrication) and applications stages.

Chapter IV. Methods of Monitoring and Estimating the Reliability of Semiconductor Integrated Circuits

5. General Principles

In considering the methods of monitoring and estimating the reliability of semiconductor integrated circuits, it must be remembered that reliability is one of the most important properties of their quality. For this reason, quality control is at the same time a method of checking the reliability of the IC's being monitored.

TABLE 11. Costs of Reliability Tests for Semiconductor IC's

(1) Количество испытываемых микросхем, шт.	(2) Допустимое количество отказавших микросхем в партии, шт.	(3) Подтверждаемая λ-характеристика с p*=0,9			
		λ=10⁻⁴ч⁻¹ hr⁻¹		λ=10⁻⁷ч⁻¹ hr⁻¹	
		Продолжительность испытания, (4) ч	Стоимость испытания, (5) тыс. руб.	Продолжительность испытания, (4) ч	Стоимость испытания, (5) тыс. руб.
10	0	2300	—	2000000	—
	1	3900	—	4000000	—
	2	5300	—	5000000	—
100	0	230	5,0	230000	4000
	1	390	7,5	400000	6000
	2	530	10,5	500000	9000
1000	0	23	12,0	23000	400
	1	39	12,5	40000	600
	2	53	13,0	53000	900
10000	0	About 2 Около 2	Approx. Примерно 120,0	2300	160
	1	Около 4	Примерно 120,0	4000	180
	2	Около 5 About 5	Примерно 120,0	5300	210

Key:
1. Quantity of IC's being tested, items;
2. Permissible number of failed IC's in a batch, items;
3. Confirmed λ characteristic with p* = 0.9;
4. Test duration, hours;
5. Test cost, thousands of rubles.

The highly reliable nature of semiconductor IC's is responsible for the insignificantly small number of device failures during even the most extensive testing, because of which the use of methods of monitoring and evaluating reliability based on the determination or confirmation of a specified λ characteristic proves to be unacceptable in the majority of cases because of economic considerations and by virtue of its excessive operating time requirements. The data cited in Table 11 which characterize the time needed to evaluate IC reliability in this way, as well

as its cost, speak for themselves. It must be kept in mind that these are clearly understated data, since in figuring the cost of the tests, only the costs of the samples being studied was taken into account (taken as equal to 10 rubles), as well as personnel salaries and overhead; such important components as the cost of the testing and measurement hardware, equipment and production space amortization, expenditures for materials and electrical power, etc. were not taken into account. Nonetheless, the data cited here are sufficient to convince one that even the most economic testing plans are burdensome financially and unacceptable because of the delay in obtaining the information needed for quality control. In essence, it is equally impossible to lose thousands of hours waiting for the results of tests necessary to make the decisions to ship or not to ship the manufactured product, or having shipped it prior to the completion of the tests, several thousand hours after finishing the tests to then take steps directed towards improving the quality. In this case, such belated information on the quality of manumfactured products carries a very expensive price. If one additionally takes into account the fact that the estimate of the reliability obtained in such an expensive way applies only to a definite type of IC, and it is not always possible to extrapolate the results obtained to other types of IC's, the inexpediency of such an approach to reliability evaluation becomes obvious [92, 93].

Another serious drawback to the method treated here is the technical complexity of the tests. The complexity of the tested unit is responsible for the complexity of the equipment used for the tests. Automated production lines, precision measurement hardware and test stands of the most complex designs as well as climatic chambers comprise the equipment of microelectronics enterprises and provide for great precision in setting production process and test modes and conditions, maintaining them and recording the measurement results. With all of this, errors are not permitted in the measurement of the parameters, otherwise, a nonexistent (false) failure will be taken into account, or, vice-versa, a real failure will be allowed. In both cases, the time and money prove to be spent in vain. It must be noted that in step with the further refinement of individual technological operations, the imperfection of which at the present time serves as a source of IC failures, their reliability will approach their own physical limit and the indicated difficulties in evaluating the level of reliability attained will increase.

The methods of monitoring and evaluating IC reliability employed in worldwide practice take these difficulties into account. Thus, for example, the military specification standards of the U.S. and other foreign nations provide for a differentiated approach to the solution of the given problem. In accordance with the documents, production monitoring is accomplished at an easily monitored level (for example, the basis for the U.S. monitoring plan is the requirement that a figure of λ = 10--20 %/1000 hr be confirmed), while no estimation is made of the attained level of reliability according to these documents. It is achieved by taking into account the data on IC reliability during operation.

By monitoring the constancy of the production level over the time segment of interest, confidence is gained that the reliability of the product batches fabricated during this period is no worse than a specified level. In other words, it is altogether sufficient to monitor the failure free rate during series pro-

duction (in contrast to trial production, when obviously it is expedient to determine both the no-failure operation figure and the service life).

Thus, the high reliability of semiconductor IC's renders an evaluation of their reliability by means of testing of little promise. The solely acceptable method of solving this problem is gathering and processing the results of IC operation. A role is set aside for tests though in check operation which is performed in the interest of obtaining information which characterizes the stability of the production process and the production level during the time segment being monitored.

Confidence in the correctness of implementing the technology and the requisite quality of the raw materials, semi-finished products and complete product assemblies, along with knowledge of what reliability the given technological process assures create the prerequisites for an apriori estimate of the reliability of integrated circuits produced over the time segment which was studied.

The product quality control system employed in worldwide practice is based on the following principles:

--In the process of doing the scientific research and prototype design work, limit tests are performed, while operational monitoring is carried out during the production process of fabricating the integrated circuits;

--Each production batch of IC's is subjected to acceptance tests, based on the results of which a judgment is made concerning the possibility of delivering this product to the consumer; standards are employed in the acceptance tests which are many times greater than the operational norms;

--The level of operational loads simulated under laboratory conditions is chosen as close as possible to the actual ones which it is still possible to reproduce using the test equipment;

--Depending on the fabrication quality, the finished products are differentiated with respect to reliability categories; corresponding to each category are its own requirements and check operations;

--The shipment of the products is based on the results of checking the production level of reliability;

--The estimate of the attained reliability level is made on the basis of results of comprehensive tests performed for the full volume, needed to determine the quantitative indicators for reliability, service life and strength safety margins as well as the safety margin for exposure to environmental factors, taking the operational data into account.

The most important features of a progressive quality control system can be characterized as follows:

--The requirements placed on the components are as close as possible to the actual ones, taking economic expediency into account: the cost of reliability assurance programs for the supplier and the consumer are taken into account;

--Test procedures are based on intensifying the developmental processes of hidden production defects and identifying failures, and provide for maximum rejection of all "weak" devices;

--During acceptance testing, product quality is checked with respect to all major requirements;

--The most progressive test procedures and the analysis of failed products are standardized;

--The engineering and standard setting documentation provides for sharing the responsibility for quality assurance and maintaining the reliability of IC's during production and operation.

The engineering standards setting documentation establishes several levels of IC quality, which differ from one another in the degree of stringency of the requirements placed on quality and the quality evaluation criteria. In line with existing practice, the norms adopted for checks at various production stages are made significantly stricter than the norms used when quality control testing the finished product. This is done in the interests of providing guarantees of the rigorous performance of production process operations and the high quality fabrication of the products in all stages.

For IC's intended for delivery to especially important projects, special reliability assurance programs have been developed. They take into account the operational conditions of the integrated circuits. The monitor operations which are repeated and targeted as much as possible towards a specific goal provide for checking that the samples being studied conform to the requirements placed on them. For example, it is well known that the U.S. space research program includes general and special programs for space systems reliability support as a whole as well as for individual equipment, assemblies and components of radioelectronic hardware.

Integrated circuits, just as other kinds of equipment components which are intended for these kinds of projects, are certified by means of performing qualification tests which guarantee the evaluation of definite reliability levels for the IC's, and are incorporated in the listing of products authorized for applications in special equipment.

During the process of IC fabrication, its quality is repeatedly and carefully checked. Beginning with the input quality control of the raw materials, semi-finished products and complete product sets and concluding with the quality control of the finished product, integrated circuits are constantly under the observation of shop workers, as well as the workers of technical control departments and reliability services.

The monitor operations during the production process for semiconductor integrated circuits comprise about 40 percent of all operations. The fraction of the outlays for monitor operations reaches 60 percent of the overall expenditures.

The numerous check operations are called upon to test the fabrication quality of the integrated circuits at various stages in the production process. In this case, checking is done to see that the following major requirements are met:

--Conformity of the external appearance of the chips, plates and bases of the IC's to the requirements of the engineering standards documentation;

--The absence of varnishes, glue and other organic materials inside the package, which are not authorized by the engineering standards documentation, as well as foreign particles;

--The absence of cracks, cuts, dirt and foreign materials over the length of the IC leads;

--The strength of the internal connections.

The quality of IC's during the production process is monitored by means of measuring the corresponding characteristics and parameters, as well as by means of all possible kinds of tests.

For ongoing monitoring of the production level and quality of the product at various stages in the fabrication, tests are employed, the kinds and order of performance of which are set forth in later sections. Recent years have been characterized by the wide scale dissemination of nondestructive techniques for quality control, estimation and prediction of reliability as well as apriori methods of predicting the reliability and durability of intergrated circuits.

Integrated circuit quality control provides for establishing the fact and degree of IC conformity to the requirements of the engineering standards documentation which regulates the requirements, norms, methods, means, procedure and organization for the conduct of tests, measurements, as well as acceptance and shipment rules for the received product. Such engineering standards documents include state and sectoral standards, enterprise standards, model regulations and technical specifications [94, 95].

The conformity of IC's to the requirements of the engineering standards documentation is evaluated by means of measurement and the determination of various parameters and characteristics under various environmental conditions under specific loads.

The listing of the parameters to be monitored during the production process is indicated in the routing charts, while the parameters of the finished products are indicated in the technical specifications.

In the interest of providing for maximum quality control effectiveness (also including economic effectiveness), the most informative parameters are chosen as those to be monitored. These are those parameters which correlated well with other ones and most fully reflect the physical processes in the IC which occur under the applied load and with the ambient conditions, as well as the variation in the processes. An effort should be made to see that their number is as small as possible. An obligatory requirement placed on the parameters selected for IC quality control is measurement simplicity, convenience and safety and the capability of reproducing the measurement results. The listing and number of such parameters are governed by experience with the design, fabrication and operation of the integrated circuits. The list of the parameters being measured

can be supplemented based on the operational results for the IC's. If failures are repeatedly found which are due to the inability to check a given parameter during production, it is essential to incorporate an additional quality control operation.

The volume of checks is curtailed if the accumulated experience attests to the expediency of eliminating particular checks.

The quality control is realized by performing the following:

--Qualification tests (in the stage of getting the products in production), the purpose of which is to demonstrate production readiness to manufacture products which meet the requirements of the customer;

--Input quality control of the materials, semi-finished products, component products and devices;

--Operational quality control of the manufacturing of the IC's;

--Monitoring the production processes;

--Quality control testing of the finished product.

The tests are performed on special equipment which assures that the specified test mode will be maintained for the requisite time and the estimation of the test data will have the requisite precision. Meeting the indicated conditions assures obtaining reliable results as well as the reproduction and uniformity of the test modes at various times on various equipment. Just as important a role is assigned to the choice of the type of test hardware as to the selection of the optimum testing procedure in the efficiency of evaluating quality.

The requirements placed on the choice of the optimal testing methods and equipment provide for the observance of the following main recommendations. They should make it possible to obtain exhaustive and objective data on the tested quality property of the integrated circuit being tested in the most economical manner. In other words, a reliable estimate of the capability of the test subject to stand up to the test conditions and maintain operability under these conditions should be obtained in the shortest possible time while using comparatively simple test equipment and gauging the minimum possible number of servicing personnel.

In cases where stand tests do not make it possible to obtain the requisite information, the results of full scale and objective tests of the IC's are employed. Objective tests of integrated circuits are nothing more than their operation as part of equipment designed around them under conditions stipulated by the technical specifications for the unit. By carefully taking into account the information on IC behavior under operational conditions, the most reliable estimate of IC reliability is obtained without additional expenditures of time and money.

A typical program for worldwide practice in acceptance testing is shown in Table 12 as an example.

TABLE 12.

Kind of Tests	Test Mode and Conditions	Greatest Permissible Percentage of Defective Devices in a Batch or $\lambda \cdot 10^{-5}$ hr^{-1}, for P* = 0.9	Acceptance Number, Items
Subgroup I		20	5
Checking the overall dimensions	In accordance with the technical specifications		
Subgroup II		20	1--5
Resistance to exposure to the soldering temperature	The IC leads are simultaneously or alternately immersed for 10 sec in solder at a temperature of +230° C to a depth of 1.5 mm from the package		
	Number of immersions is indicated in the technical specifications		
Thermal cycling	From -65° C to +175° C. Exposure time 30 min; transfer time 5 min. Number of cycles: 5.		
Thermal shock	From +100° C to 0° C. Exposure time 0.25 to 5 min. Transfer time 3 to 10 sec. Number of shocks: 5.		
Moisture resistance	From -10° C to +60° C. Moisture up to 98%. Time for 1 cycle, 24 hr. Number of cycles indicated in technical specifications.		
Subgroup III		10--20	2--5
Multiple shocks	Acceleration of 1,500 g; pulse width of 0.5 msec, 5 shocks each in 3 mutually perpendicular directions. Overall number of shocks: 15.		
Vibration strength at a fixed frequency	Frequency of 60 Hz; acceleration of 20 g; 32 hr each in 3 mutually perpendicular directions. Total testing time: 96 hr.		
Vibration strength in a range of frequencies	Frequency of 100--2,000 Hz; acceleration of 20 g; testing time: 48 min.		

TABLE 12. [cont.]

Resistance to the action of a constant (centrifugal) acceleration	Acceleration of 20,000 g; 1 min each in 3 mutually perpendicular directions. Overall testing time: 3 min.		
Subgroup IV		20	1--5
Checking the mechanical strength of the leads	Three leads are checked by means of suspending a load. The weight of the load and the time are given in the technical specifications.		
Subgroup V		20	1--5
Checking the corrosion immunity	The devices are kept for 24 hr in a chamber with a salt fog at T = +35° C. The concentration and flow rate of the fog should provide for a salt precipitation of no more than 50,000 mgm/m^2 per 24 hr.		
Subgroup VI		λ = 10--20	-
Storage	T = +175° C; duration of 1,000 hr.		
No-failure operating time	T = +125° C; duration of 1,000 hr. Nominal electrical mode.		
Subgroup VII		λ = 10--20	-
No-failure operating time	T = +125° C; duration of 1,000 hr. Nominal electrical mode.		

As follows from Table 12, the various kinds of climatic and mechanical tests are combined into individual subgroups. The products are subjected to these tests in a definite sequence. In accordance with the selected plan for selective monitoring, corresponding to each subgroup of tested samples is its own acceptance number, which expresses the permissible number of failures or the specified failure rate. The results of tests are considered satisfactory if the number of integrated circuits (IC's) which failed during these tests does not exceed the established norms.

Production monitoring of the established reliability level is accomplished by means of tests for failure free operation, while the estimate of the attained

reliability level during the average service life is found by means of testing the IC's for operating longevity. Tests for failure free operation solve the problem of determining the probability of no-failure operation or the failure rate during the specified continuous testing time. Longevity tests make it possible to determine the reliability of the tested circuits over the course of the guaranteed service life.

The volume of the tests is determined in strict accordance with the purpose of the tests. If the issue is the performance of production checks of the reliability of the output product for the purpose of determining production stability, then in selecting the sample size and the testing duration, one should proceed primarily from considerations of the maximum assurance of operational timeliness of the quality control and economic substantiation of the selected testing plan. The main factor in the determination of the reliability estimate is assuring the requisite confidence level of the results.

The most acceptable plan in all respects for ongoing reliability monitoring is a monitoring plan based on two specified reliability levels [92,96].

Such a plan is based on monitoring the constancy of a minimum reliability level, P_{min}, taking into account the acceptable level, $P_{пр}$ [P_{acc}], which is agreed upon by the manufacturer and the customer and provides for observing the interests of both parties. Selective quality control plans based on two levels have been described in detail in the literature [96-99]. Because of their advantages, they find widespread applications in many sectors of industry.

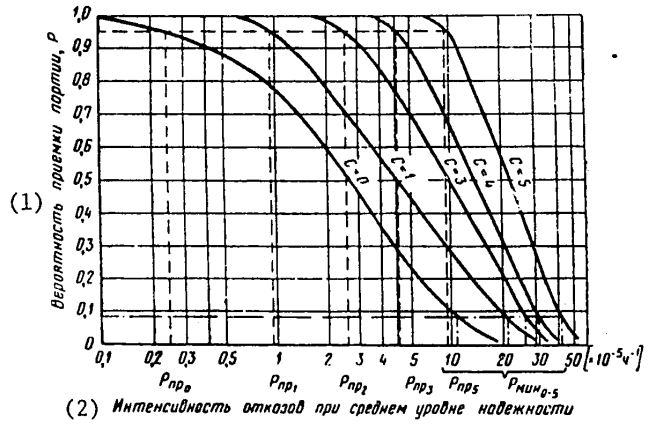

Figure 22. Family of operational characteristic curves for a selective monitoring plan with two levels of reliability.

Key: 1. Probability of batch acceptance
2. Failure rate at the average reliability level.

The essence of selective quality control with respect to two levels consists in the following. Working from the proposed or attained reliability level, which is taken as the acceptable level P_{acc}, a minimum reliability level P_{min} for the case of a specified value of manufacturer's risk α, where the constancy of P_{min} is monitored during the testing process for the case of a specified consumer risk β. The requisite sample size, n, and the acceptance numbers, c, are determined on the basis of the established levels. For small acceptance numbers (c = 1--3), the difference in the values of P_{acc} and P_{min} fluctuates from 6 to 13. Production monitoring at a level of 6 to 13 times lower than the attained level makes it possible for the manufacturer to test a small number of devices in a short time, something which makes these tests economically advantageous. The interests of the consumer are covered in this case (with a risk of β of receiving poor quality products) with a confidence that in (F) $1 - \beta$ cases, the received products will have a reliability above P_{min} at least as much as is required so that the manufacturer's risk α (the risk of rejecting a good product) does not exceed the established level. Thus, the constancy of P_{min} will be evidence of the maintenance of the reliability of the output product at the requisite level. The family of operational characteristic curves for the selective quality control plan based on two levels is shown in Figure 22, which clearly reflect the probability of accepting (or rejecting) products as a function of their reliability.

The use of supplemental samples is permitted during the quality control process, the size of which is governed by the difference between the sample corresponding to the main plan, and the sample in accordance with the equivalent plan. In this case, the total number of failures during device testing should not exceed the acceptance number for the main plan.

The manufacturer, in basing his work on definite production process margins, is himself correct in choosing a more stringent plan than the plan specified by the consumer, and implementing quality control at a higher level of reliability. If the actual reliability level proves in fact to be the one for which the tests are passed successfully, their results will be just as objective as the positive results of tests in accordance with the main plan, while the cost will be lower.

Equivalent plans make it possible where production is well set up to successfully implement quality control with smaller samples and improve the economic indicators of production.

When checking and evaluating the reliability of such difficult to monitor products as integrated circuits, failure analysis is of critical importance. Production reliability monitoring of current products and the apriori estimation of the reliability level can be based on the failure distribution for various circuit tests. In particular, this applies to climatic and mechanical tests which in and of themselves do not allow for the quantitative estimation of product reliability. The failure distributions with respect to the kinds of failures and types of tests obtained in the testing process are compared with the corresponding distributions of previously tested batches, the reliability of which was acknowledged as satisfactory. If the distributions match, it can be assumed that the quality, and consequently also the reliability of the given batch is no worse than for the

products tested earlier. A significant divergence between the obtained distribution and that adopted as the reference standard can be evidence of the appearance of a new failure source and mechanism. In this case, the given batch of circuits is carefully analyzed and the source of the failure is determined and eliminated.

The utilization of this method for production monitoring and apriori estimation of IC reliability is possible only with an established technology for their fabrication. It is important in this case to know what level of circuit reliability is provided by the given technology and to strive to assure that it is constantly observed during the circuit manufacturing process.

Reliability Estimation. Integrated circuit reliability is estimated under production conditions in accordance with the documentation which is in force by means of testing the circuits for longevity, taking into account the results of operating equipment using the integrated circuits. The plan for conducting the

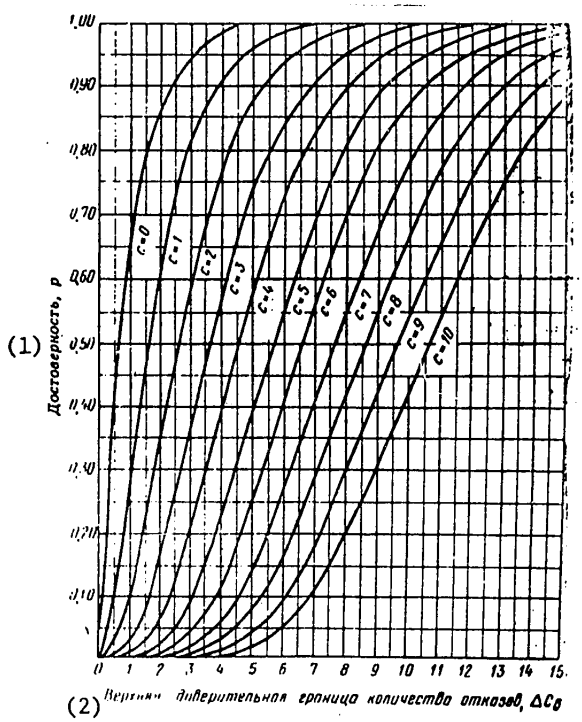

Figure 23. Curves for estimating the reliability of products with various confidence levels of the estimate.

Key: 1. Confidence level, p;
2. Upper confidence limit of the number of failures, ΔC_B.

longevity tests is set up by working from the formulated task: confirm the anticipated reliability level or determine the actual reliability over the course of a specified service life. When determining sample size, one works from the requisite confidence level with which results must be obtained. Curves are plotted in Figure 23 which show how the test results (the upper boundary of the confidence interval) depend on the confidence level. By using this graph, one can determine the requisite sample size by means of formulas (8)--(10) or the relevant tables given in the literature [96--98].

The quantitative reliability indicators are calculated assuming an exponential distribution of the failures, using the well known formulas:

$$\lambda_{on}(t) = \frac{c}{nt}; \tag{8}$$

$$\lambda_{B}(t) = \frac{\Delta c_{B}}{nt}; \tag{9}$$

$$\lambda_{H}(t) = \frac{\Delta c_{H}}{nt}; \tag{10}$$

$$P(t) = 1 - \lambda t, \tag{11}$$

where λ_{on} is the test value of the failure rate, hr^{-1};
λ_B and λ_H are the upper and lower confidence interval limits respectively for the values of the failure rate with a confidence level of P*, hr^{-1};
c is the number of units which failed over a time t, items;
Δc_B and Δc_H are the reduced values of the number of units which failed over the time t, corresponding to the upper and lower bounds of the confidence interval;
n is the number of units good at the start of the time interval under consideration, items;
t is the time interval being analyzed, hr.

The data of Table 13 can be used to determine Δc_B and Δc_H where P* = 0.9.

An important role in estimating IC reliability is assigned to the information obtained in the course of operating radioelectronic equipment designed around the IC's. The special role of operational data when figuring IC reliability is determined by two major principles: first of all, by the fact that it is specifically these reliability indicators which are required for practical utilization in calculations of the reliability of radioelectronic equipment being designed; and secondly, by the difficulties in estimating the attained high reliability by means of tests by the manufacturer.

One of the ways of overcoming these difficulties is using all of the information acquired over the time interval preceding the point in time of the estimate. Utilizing operational reliability data, as well as the results of longevity and no-failure service tests, production process tests and the results of studying IC reliability using special programs makes it possible to increase the confidence level of the estimate of the attained reliability level.

TABLE 13.

(1) Количество отказавших образцов c, шт.	(2) Односторонний интервал $\Delta c_в$, шт.	(3) Двусторонний интервал $\Delta c_н$, шт. items	(3) Двусторонний интервал $\Delta c_в$, шт. items	(1) Количество отказавших образцов c, шт. items	(2) Односторонний интервал $\Delta c_в$, шт.	(3) Двусторонний интервал $\Delta c_н$, шт. items	(3) Двусторонний интервал $\Delta c_в$, шт. items
0	2,30	0,00	3,00	6	10,53	2,61	11,84
1	3,89	0,05	4,74	7	11,74	3,29	13,15
2	5,32	0,35	6,30	8	12,99	3,98	14,43
3	6,68	0,82	7,75	9	14,21	4,70	15,71
4	7,99	1,37	9,15	10	15,40	5,43	16,96
5	9,27	1,97	10,51				

Key: 1. Number of failed units, c, items;
2. One-way interval, Δc_B [upper], items;
3. Two-way interval.

The following expression is used when calculating the quantitative reliability indicators based on several tests of batches:

$$\lambda(t) = \frac{\sum_{i=1}^{m} c_i}{\sum_{i=1}^{m} n_i t_i}, \tag{12}$$

where c_i, n_i and t_i are the number of units which have failed, the number of units good at the start of the tests and the testing time for the i-th sample respectively.

The mean statistical value of the failure rate in the case of an exponential distribution can be determined from the formula:

$$\lambda_{ст} = -\frac{2{,}3 \lg P_{ст}}{t}, \tag{13}$$

where P_{CT} is the mean statistical value of the failure free operating probability over the time t.

$$P_{ст} = \frac{\sum_{i=1}^{m} n_i P_{оп i}(t)}{\sum_{i=1}^{m} n_i}, \tag{14}$$

where n_i is the i-th sample;
m is the number of samples;
$P_{оп i}$ is the test value of the probability of failure free service of the i-th sample;
$P_{оп}(t) = 1 - (c/n)$ (15)

$$P_{оп}(t) = 1 - \frac{c}{n}.$$

when $P_{CT} \geq 0.9$,

$$\lambda_{CT} = \frac{1 - P_{CT}}{t}. \tag{16}$$

The results of non-failure operating tests performed within the framework of the production quality control for output product reliability are used to estimate the reliability.

No-failure operation tests are performed in a forced electrical mode at an ambient temperature of +125° C. As follows from the graph (see Figure 7), the failure rate at this temperature averages 13 times higher than at normal temperature. Using an acceleration factor of $K_y = 13$, makes it possible to obtain a value of the failure rate of no more than $\lambda = 2.2 \cdot 10^{-6}$ hr^{-1}. Thus, even a small volume of no-failure operation tests can be used to determine the achieved level of reliability.

The objectivity of the estimate will increase in step with the generalization of the results of the periodic monitoring of the reliability.

An analysis of the existing domestic quality control and reliability assurance system for integrated circuits shows that the system of documents which regulate the requirements placed on quality, as well as the norms and methods of reliability and quality control encompass to an insufficient extent the existing capabilities for further improving the efficiency of efforts in this area.

However, there are still also deficiencies in the organization of IC quality control. A number of methods and standards for IC tests in accordance with additional consumer requirements and programs which reflect specific conditions of product applications have not as yet been standardized.

The IC quality control system which is in wide use is also inadequately effective because it does not provide for complete utilization of the information on the manufacturing quality of products and reliability under operational conditions [99]. In contemporary production, of all of the information obtained during quality control and reliability checking of integrated circuits, only that part of it is taken into account which is essential for estimating the suitability of the finished product and for making decisions concerning its shipment to the customer.

This occurs primarily as a consequence of the lack of a strict quality control system for products during their manufacture, and in particular, because of a lack of automated control systems which provide for data analysis, storage and feed-out at the necessary time, where this information is needed to correct the production process, as well as for test program comparison and other standard setting engineering documentation, which regulates the methods and procedures for production control for the purpose of assuring output products of a specified quality.

In the literature which has been cited, the deficiencies of the existing testing system have been formulated as follows:

1) The development of testing programs without considering the results of the tests of the entire preceding aggregate of output products and the introduction of special methods of IC quality control in individual operations based on the results of quality monitoring; 2) the failure to use the results of operational quality control when planning tests; 3) the failure to receive information on time, due to primarily to the use of manual labor in the monitor operation and when processing the test results; 4) a low confidence level for the quality estimate in the majority of cases, which is explained by the lack in a number of cases of scientifically substantiated standards and requirements placed on the test modes, the precision in setting and maintaining them as well as by the methods of carrying out the measurement operations used in this case and the reference standard base. All of this leads to the necessity of repeated tests, which unavoidably entail an increase in the cost of production, the product, and an extension of the time frames for placing the products in production and manufacturing them.

Replacing the existing product reliability and quality control system in microelectronics with an automated quality control system (ASUK) is the only way of eliminating the deficiencies and further improving production efficiency. In order to justify the hopes placed in it, an automated quality control system should be based on the creation of the techniques and hardware for metrological, engineering, technical, software, informational and organizational support.

One of the possible variants for an automated quality control system structure is treated in [99], which provides for shifting the center of gravity from the monitoring of the finished product to more careful and exhaustive operationally timely monitoring. The author of the proposed system notes with justification that in the early stages of integrated circuit design, quality control of the fabrication is more effective, since there is the real possibility there of preventing the appearance of defective products.

Along with this, tests of the finished product remain the only way of obtaining the information needed for a final quality evaluation of the produced product. For this reason, control of the tests is one of the major tasks of an integrated circuit automated quality control system. Testin control is understood to be the development and realization of a set of organizational, technical and scientific and procedural measures, which provide for the preparation and conduct of the tests (planning the preparation, selecting the testing plan, the test operations, the analysis of the results obtained and working out the corrective actions to take in production).

6. The Classification of Tests

Integrated circuit quality is composed of a number of properties which characterize circuit functional capabilities (resorption time, ultimate temperature, characteristics of the major structural components which govern the integrated circuit parameters: base, collector and emitter currents, leakage current, junction capacitants, dynamic resistance between the emitters, forward voltage drop across the collector--base junction, inverse voltages across the collector--

base and emitter--base junctions, residual emitter--collector voltage, etc.), the operational capability (heat resistance and thermal stability, moisture resistance and operating stability in the presence of moisture, cold resistance and operational stability in the presence of cold, vibrational strength and vibrational stability, shock strength and operating stability under shock loads, strength in the case of free fall and transportation, resistance to centrifugal acceleration, etc.) as well as durability, non-failure operating life and shelf life. The structure of integrated circuit quality is shown schematically in Figure 24. Among these properties there are a number of properties (weight, hermetic seal integrity, lead strength) which characterize the fabrication quality of each integrated circuit taken individually.

As is well known, reliability is one of the major quality properties of any product, and integrated circuits in particular. It characterizes the capability of an IC of performing its own functions under definite conditions for a specified time. Integrated circuit reliability is conditioned by its non-failure operating time, durability, and shelf life [100]. Non-failure operating and durability of a microcircuit determine its capability of maintaining operability for a specified time. This difference between these concepts consists in the fact that the former provides for the retention of operability for a specified time interval without interruptions in operation, while the second provides for the retention of operability until completely worn out, with interruptions in operation for technical servicing and repair. The non-failure operating probability and failure rate serve as the non-failure operating time indicators. The durability indicators are the average service life of the integrated circuits, the minimal mean time between failures and the gamma percentage service life.

Shelf life of an IC is the property of the IC of preserving the stipulated operational indicators during and after storage and transportation, the duration and conditions of which are established by the engineering standard setting documentation. The shelf life indicator for integrated circuits, in particular, is the average storage life.

All of these properties of IC quality are specified in the technical specifications and are subject to check with a definite accuracy.

Measurements and tests are the only source for obtaining objective information on integrated circuit quality. By simulating the environment under laboratory conditions, the IC's being studied are exposed for a definite time to various operational loads and in this way, a rather precise idea (close to the actual value) is obtained concerning the resistance, strength and immunity of integrated circuits to these factors, the extent of the influence of the load on the structure of products and the capability of a unit being tested of standing up to the destructive effect of the ambient temperature, vibration, radiation, dust, humidity, pressure, etc.

The engineering standard setting documentation provides for the performance of the following kinds of tests when checking the quality and reliability of IC's:

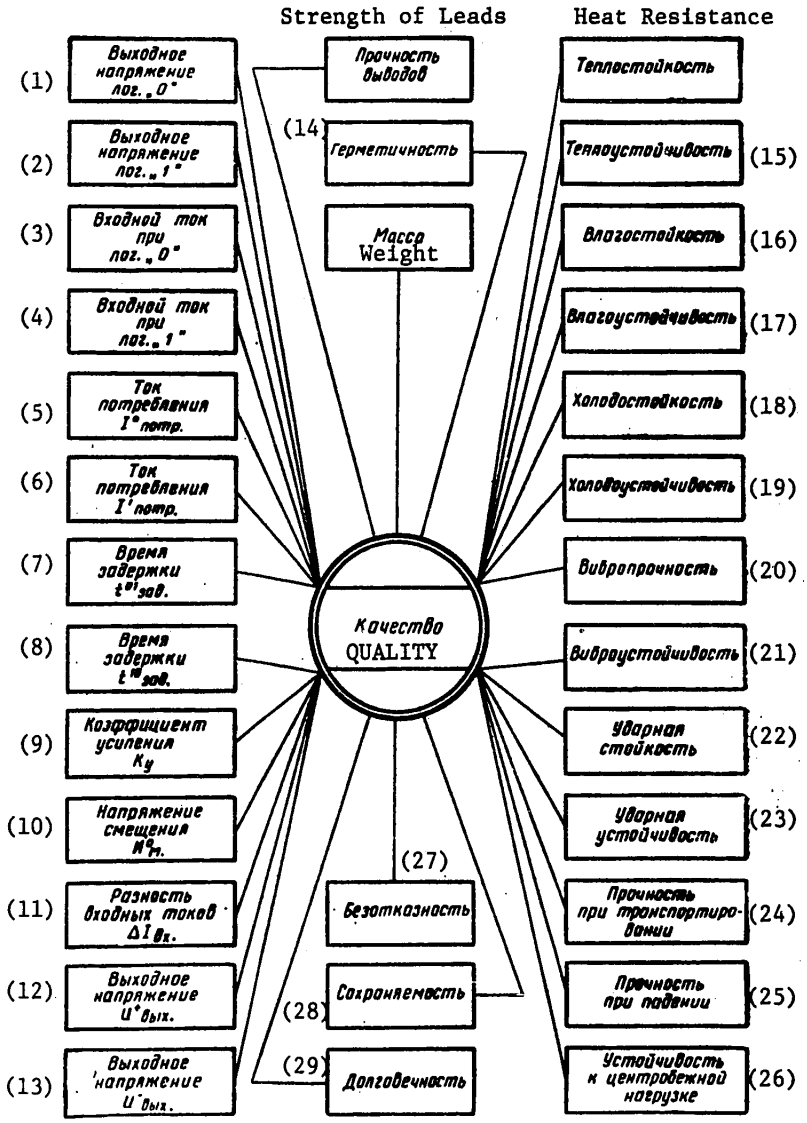

Figure 24. Typical block diagram of the quality properties of a semiconductor integrated circuit.

Key:
1. Logic "0" output voltage;
2. Logic "1" output voltage;
3. Input current for a logic "0";
4. Input current for a logic "1";
5. Current consumption, I°_{cons};
6. Current consumption, I'_{cons};

7. Delay time, $t^{01}_{del.}$;
8. Delay time, $t^{10}_{del.}$;
9. Gain, K_y;
10. Bias voltage, U^0_M;
11. Difference in the input currents, ΔI_{in};
12. Output voltage, U^+_{out};
13. Output voltage, U^-_{out};
14. Hermetic seal integrity;
15. Thermal stability;
16. Moisture resistance;
17. Operational stability in the presence of moisture;
18. Cold resistance;
19. Operational stability in the presence of cold;
20. Vibration strength;
21. Operational stability in the presence of vibration;
22. Impact strength;
23. Operational stability in the case of shock loading;
24. Strength during transporting;
25. Strength in the case of a fall;
26. Resistance to centrifugal loading;
27. Non-failure operating time;
28. Shelf life;
29. Durability.

1) Mechanical tests to detect resonant frequencies, vibrational strength, stability under vibrational loads, impact strength when exposed to one-time and repeated shocks, resistance to single shocks, strength when exposed to centrifugal accelerations, lead strength (tensile strength, bending strength, bending fatigue strength) and the strength of the internal connections;

2) Climatic tests for heat resistance and thermal stability, cold resistance and operating stability in the presence of cold, storage life at an elevated temperature, resistance to a cyclical temperature variation, resistance to heat shock, moisture resistance and operational stability in the presence of moisture, stability at reduced atmospheric pressure, operating stability and resistance to the effect of environmental factors at the due point and exposure to hoar frost;

3) Acoustical tests for resistance to sound pressure (to a single noise);

4) Biological tests for resistance to the development of mold and fungi;

5) Electrical tests for insulation resistance, non-failure operating time, durability and service life;

6) Chemical tests for explosion hazard, suitability for soldering, resistance to corrosion when exposed to a corrosive medium;

7) Hydrolic and pneumatic tests for the effect of an elevated air pressure, the effect of barometric shock and the hermetic seal integrity;

8) Flammability tests.

The classification cited here was compiled taking into account the requirements of [101]. However, one must point out the fact that the cited standard does not fully reflect worldwide experience and the industrial sector standard setting engineering documents. In turn, the latter do not conform to the requirements of the given standard. For this reason, the authors considered it possible to employ the classification which was acceptable at the same time both for the presentation of the given material and on the whole for the problems of testing devices, equipment and components. It is impossible to justify the presence of two individual, independently existing classifications for tests: tests of devices and equipment, and tests of electronic hardware products.

We shall consider the specific features of the classification which is discussed in the book.

It is difficult to imagine a classification which would not provide for a gradation of the tests, depending on the step in the manufacture of the product. Such differentiation exists in principle in [101], but in a very veiled form and is in need of being made more precise. In accordance with this standard, there exist research and operational tests. The first are performed primarily in the stage of working out the draft plan of the product, while the second, as follows from the name, are performed during the operation of the finished product. In practice, these are most frequently the operation of the product for testing or physical unit tests. However, tests performed during the production stage are lacking in the table of the standard as an independent category, something which is responsible for the lack of clarity and the incomplete nature of the testing classification with respect to this first and most important criterion. Technological production process tests are lacking among the production tests cited in the standard which are performed during the product fabrication stage. This kind of testing is especially important for industrial sectors which produce electronic equipment products. To be included in the group of production process tests are all the kinds of tests which provide for the fabrication technology of a product at various stages in the production process and which pursue the goal of step by step checking for the formation of the specified product properties.

Tests which in engineering practice are called conditioning, rejection, production process run, burn-in, artificial aging or "seasoning" tests, etc., or completely undeservingly bypassed by the standard [101]. These are very important kinds of tests, which are widespread in industrial sectors producing electronic and electrical equipment products. Burn-in or rejection tests are performed for the purpose of ascertaining and rejecting from the manufactured products the defective, potentially unreliable product units. Another task of these tests is to increase the operational stability of the conditioned products and reduce the scatter in the values of the product parameters, in the general set of products, which in this case is IC's. Such tests provide for a substantial increase in product quality while simultaneously increasing the plan income of an enterprise [4, 27, 102] and cannot but occupy a necessary place among the other kinds of tests. It can be assumed that not all quality control specialists are in agreement in including conditioning among tests instead of including it among

production process operations. Such a viewpoint has a right to exist and can be discussed. We include these kinds of tests among the group of production process tests, working from the duality of their nature: on one hand, the formation of definite quality properties in a product, and on the other, the purely checking functions performed by the test procedures using the test equipment.

Another deficiency of the standard of [101] which is especially important for classifying the tests of devices and equipment is the lack of a criterion among the classification criteria which characterizes the status of the unit being tested: breadboarded unit, trial or prototype unit subjected to testing or a series and mass produced product which is being tested.

The classification of tests within the limits of the criteria provided in [101] is also not optimal and is in need of improvement.

Thus, for example, by working from the definitions given in the main text of this standard setting engineering document, all of the tests can be subdivided according to the purpose for which they are performed into research, check, comparison, determination, developmental debugging, certification, service life and reliability tests. It appears erroneous to merge research and comparison and check and developmental tests into a single group. Research tests can be both comparison and determination tests. One can also include developmental tests in the group of research tests, since in accordance with the standard, these are "tests performed in the process of developing a product to evaluate the impact of changes made in it for the purpose of attaining the requisite quality indicators."

A more precise formulation is given in the reference appendix to the standard under discussion here. In accordance with the classification given in the appendix to standard [101], all of the tests are broken down according to the purpose for which they are performed into check, research and limit tests. However, in our opinion, this explanation too does not make the classification finally complete. Differentiation of tests into research and check tests is logical. The presence of limit tests in this group is not justified. According to the definition given in the main text of the standard, limit tests are research tests and for this reason cannot appear together. The standard includes a definite portion of the test types in the category of check tests. Exceptions are determination tests, which "can be included among check or research tests...", as well as comparison, developmental debugging, certification, accelerated tests, normal tests, stand or test facility tests, operational, destructive, nondestructive, service life and reliability tests. The association of these tests with some category or group of tests by the standard [101] is not established and their place in the classification table is not indicated.

Other positions taken by the state standard being analyzed here are also disputable. Thus, for example, the difference between comparison and evaluation tests is presented in such an ambiguous manner that it is difficult to imagine when one should be used in practice and when the other should be used.

No category is provided in the standard in which certification tests are to be included.

Approximately the same thing can be said about developmental debugging tests.

It is hardly correct to include the abbreviated tests provided in [101] among accelerated tests. The formulation of this kind of test defines them as: "accelerated tests without intensifying the processes which cause failures or damage". But in Appendix 1 to the standard, it is explained that in the case of abbreviated tests, "a reduction in the time needed to acquire the requisite volume of information can be achieved, for example, based on the use of supplemental information obtained outside the tests. . .", and then the explanation is given as to via which routes one can obtain this additional information, and among them are the application of extrapolation techniques, etc. This is already a different way of obtaining information on the property of the product being checked, which exists on an equal footing with a test, but is not a test. In this case, the intermixing of three classification criteria is present: duration, conditions for test performance (in nominal or forced modes) and the source of the original information needed to estimate the quality of the product being checked. "Accelerated tests can be either forced or abbreviated," states the standard, and it is right there admitted that so-called "abbreviated tests" may also not be tests at all.

It appears that the differentiation of the tests according to the classification criteria of "property being evaluated" and "point of performance" has not been thought through to the conclusion.

According to the first of these criteria, tests are subdivided only into reliability and service life tests. Essentially no place has been found in the standard for vibrational strength and operational stability under vibrational load, moisture resistance and operational stability with exposure to moisture, heat resistance and thermal stability tests as well as tests similar to them which are performed for a similar purpose.

According to the second classification criterion, tests are broken down into operational and test stand types. Again no place is found in the classification table for laboratory tests which the designer or the manufacturer of the product performs on test stand equipment.

The standard considered here [101] is not the only document which regulates the classification of tests and the terminology in this field. In addition to this standard, similar problems are also solved in [100, 103-105]. However, the presence of these additional documents does not bring any order to the problem under discussion. Thus, for example, in contradiction to standard [101], according to standard [104], hydrostatic, biological and radiation tests are included in the group of climatic tests, while acoustic tests are numbered in the group of mechanical tests. While according to [101] quality control tests are tests of a unit performed to monitor its quality, according to [105], these are tests of units from a set-up series and series produced products.

Acceptance tests, according to standard [101] are "quality control tests of prototype units (batches) of a product, as well as products from a single pro-

duction run, which are performed to resolve the question of the expediency of placing this product in production or turning it over for operation respectively." However, according to standard [105], acceptance tests are "tests of prototypes of new types of products, intended for series production, as well as imported products." The fact that in the example considered here the issue involved different products cannot justify the differing formulations of the same concepts, since the kind of products being tested is of no importance for the classification of the tests.

Even a unified terminology has not been worked out at the present time. Definitions of strength and resistance are encountered at each step which are used to define the capability of a product of standing up to the destructive effect of a definite load and to maintain operability and external form after exposure to this load. In contrast to the concept of "stability", which is used to characterize the capability of a product of retaining operability when exposed to this load, the term "strength" means the retention of operability by a product as a consequence of this exposure [sic].

Without doubting the obvious nature and expedience of using the term "stability", we shall put forward our own point of view concerning the terminology for describing the capability of a tested unit of retaining its qualities following exposure to operational factors. In our opinion, no effort should be made to substitute the word "resistance" for the term "strength" or vice versa.

It is convenient to use both of these terms in practical work.

Each of them under certain conditions is more suited to the description of a particular physical process. For example, when the issue is one of the capability of an IC of standing up to exposure to a corrosive gaseous medium (for example, a salt atmosphere), one does not want to talk about the "strength of an IC with respect to a sea fog", but it suggests itself to say rather "immunity . . . to a fog". The same thing must be said about other tests. The operational stability of a product in the presence of moisture sounds better than saying its moisture strength. In the case of describing the capability of a product during exposure to mechanical loads, it is equally correct, in our view, to say both vibrational strength and vibration immunity (in contrast to vibration stability). However, for the purpose of bringing order to the terminology and the rules for utilizing it, it is probably nonetheless necessary to make a choice of one of the terms. Taking into account what has been said here, the following system is proposed: to describe the mechanical strength of products, use the term "strength" (vibrational strength, impact strength or shock strength, strength in the case of a fall, tensile (or compression) strength, strength in the case of a centrifugal load, etc.). However, the capability of products of preserving their qualities and conforming to the requirements of standard setting engineering documentation following exposure to climatic, biological and chemical factors is characterized by the definitions: "moisture immunity", "corrosion immunity", "fungal immunity", "immunity (but not "strength") to cyclical temperature changes", "thermal immunity" (but not "thermal strength"), etc.

A few words are in order concerning terminology in area of testing, in which the main kind of exposure is to gas or liquid pressure. The standard [101] does not reflect the physical nature of the phenomenon and does not differentiate between atmospheric pressure and artificially produced pressure. While the first serves as a load when studying the capability of a product of operating under natural conditions, the second is a direct consequence of human activity. For this reason, it is correct to include stability testing at reduced atmospheric pressure among the group of climatic tests, since testing for exposure to elevated gas or liquid pressure is numbered among hydrolic and pneumatic tests.

Thus, test classification according to the attribute of the "kind of acting factor", employed in the given monograph, appears as shown in Table 14.

In this table, the authors present their own variant of test classification based on other attributes as well. We shall not comment on the classification table in detail because of a lack of space here. We shall only underscore the fact once again that it takes into account the deficiencies of the standard [101] as well as operational experience in the microelectronics sector of industry.

Research Tests. According to the classification of tests which is given in state standard [101], tests performed in the interests of studying definite properties of a unit are called research tests. A representative of this class of tests is limit tests. The standard definition of limit tests reads: "limit tests are research tests performed to determine the relationships between the ultimately permissible values of parameters for a product and the values of the operational mode parameters."

Tests of this kind are employed for the purpose of ascertaining the range of stable and reliable operation of a product, determining the correlation function of the parameters, establishing the listing of parameters to be checked and the standards for them, working out methods of evaluating and predicting integrated circuit reliability, as well as establishing the requirements placed on redundancy of IC components and requirements placed on the measurement and test facilities used in working with a given type of integrated circuit.

These tests make it possible to estimate the strength and stability margins of integrated circuits exposed to various factors, and to determine the distribution of product failure according to kinds and degree of severity of the acting factors.

Included among limit tests are thermal shock tests, thermal cycling, one-time large force shocks, centrifugal loading, resonant frequency tests as well as high temperature storage.

The methods for performing these tests are selected by working from the posed problem and the design and production process features of the tested unit. General rules for the performance of limit tests provide for the following:

--The performance of the tests right up to the destruction of large parts of the samples;

TABLE 14. Classification of Tests for Radioelectronic Equipment and Electronic Products

Product Production Stage	Design-nation	Purpose	Classification Attribute: Place and Manner of Performance	Classification Attribute: Status of the Unit Under Test	Nature of the Test	Manner of Evaluation	Major Acting Factor
Development	Research	Limit and debugging	Test stand and proving ground categories	Breadboarded and prototype units		Comparative	Mechanical tests Climatic tests
Production	Acceptance	Preliminary (plant); Departmental Interdepartmental State, Acceptance, turnover; Qualification	Test stand, proving ground and unit tests	Products from series and mass-production	Destructive and nondestructive	Determination	Acoustic tests Biological tests Electrical tests Chemical tests Hydrolic and pneumatic tests Flammability tests Radiation tests Electromagnetic tests Magnetic tests
	Check	Periodic Standard type Certification Quality control sampling Durability Non-failure operation Service life Mean time before failure Shelf life Input quality control Operational quality control					

TABLE 14. [Cont.]

Product Production Stage	Designation	Purpose	Place and Manner of Performance	Status of the Unit Under Test	Nature of the Test	Manner of Evaluation	Major Acting Factor
Production	Production process	Rejection Conditioning	Test stand	Products from series and mass-production		Comparative, determination	
Operational	Check	Monitored operation	Proving ground and unit tests	Prototypes, products from series and trial production	Destructive and nondestructive	Determination	

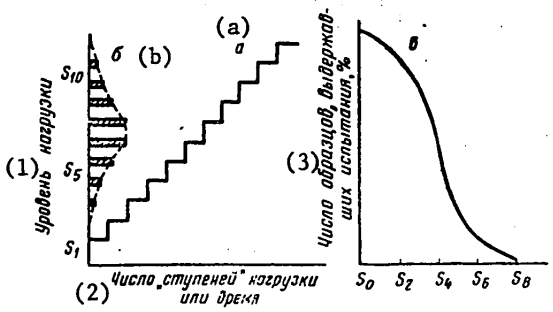

Figure 25. The change in the load (a), failure distribution as a function of the load (b) and the number of units which pass the test as a function of the load level (c).

Key: 1. Load level;
2. Time or the number of load "steps";
3. Number of units which pass the tests, percent

--Gradual increase in the load;

--The choice of the kind and size of the load so that it is not accompanied by the appearance of new failure mechanisms which are not inherent in the given type of integrated circuit during operation.

The technique of a gradual stepped increase in the load has been recognized as the most expedient and is universally used (Figure 25). A typical curve for the rise in failures during accelerated durability tests, performed using a stepped load, is shown in Figure 26. Thus, the test method treated here is based on a gradual failure of units (in step with the increasing load) which have different defects, and which under operational conditions could appear in the course of an extremely long operating time.

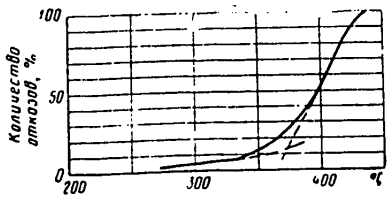

Figure 26. Typical curve for the increase in the number of failures during accelerated tests of durability (stepwise increase in the temperature).

Key: 1.Number of failures, %.

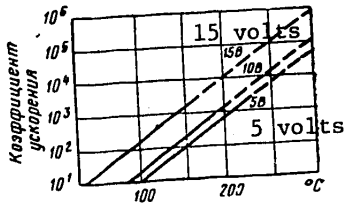

Figure 27. Graph of the change in the value of the failure acceleration factor as a function of temperature and voltage.

Key: 1. Acceleration factor.

Usually, one kind of load or another is employed. But there are cases of the simultaneous use of several loads of a different nature.

Combined exposure to two different loads makes it possible to amplify the effect and reduced the duration of the tests even more. The growth in the acceleration factor with an increase in the electrical and thermal loads applied to the product at the same time is shown in the graph of Figure 27. The resulting function reflects the results of tests of planar transistors in the reliability improvement program for the Minuteman project. The curves in the graph for temperatures above 200° C were plotted on the basis of extrapolating the experimental data of paper [4].

We shall consider the methods of performing specific kinds of tests.

The technique of limit testing using thermal shock (heat shock) is the same as with conventional testing. The difference is in the number of cycles. In the case of the limit variant, the number of cycles has no standards set for it and depends on the established criterion for evaluating the test results. The test is conventionally terminated when 50 percent of the IC's supplied for the test fail or when the integrated circuit immunity is confirmed with the reaching of the final stage of the test exposure. The number of thermal shocks is figured in tens of shocks. The ultimate values of the temperature and the periodicity of parameter measurement are indicated in the engineering standard setting documentation.

Testing by thermal cycling is accomplished by increasing the load in each subsequent step. The ultimate and intermediate values of the temperature are specified in the engineering standard setting documentation. The initial and final loads are selected by working from a consideration of the specific requirements placed on the structural design of the integrated circuits and their fabrication technology. When performing succeeding tests on integrated circuits of the same structural and production process design, the same stages are provided as in the preceding case, however, the initial step is chosen two steps below that one at which failures occurred during preceding tests.

Integrated circuit testing, which pursues the goal of determining the strength margin and the immunity to exposure to temperatures, is performed by increasing the temperature in steps. The duration of the exposure in each step is figured in hours.

The strength and stability margins of integrated circuits in the case of simultaneous exposure to the ultimate ambient temperature and electrical load are evaluated by means of a stepwise increase in the electrical load at a constant ambient temperature.

The load is increased from the nominal to the ultimate value. The duration of the exposure of the integrated circuits in each step is governed by their function and the structural design and production process features, and is indicated in the testing documentation.

In the case of tests at a constant electrical load, a value of 0.8 to 0.9 of that ultimate load which is obtained when testing with a variable load is chosen as that load.

Mechanical shock and centrifuging tests are performed by sequentially increasing the load in steps, which are specified in the engineering standard setting documentation. In this case, the products being tested are arranged so that their exposures are realized in directions which are the most hazardous for them.

Production Process Tests. Production process tests serve to check the fabrication quality of products at various stages in the production process and reject substandard products.

This very important kind of testing is not reflected in the standard of [101], has been undeservedly forgotten and not taken into account in the classification of the kinds of tests.

The significance of production process testing is extraordinarily great in all stages of integrated circuit fabrication. Input quality control of the raw materials, semi-finished products and complete product sets establishes the basis for a high quality product. Effective operational monitoring provides for the execution of all production processes in strict conformity to the standard setting engineering documentation and thereby, the observance of all the requirements placed on production. The final total of the operational quality control serves to prevent rejections when fabricating IC's and the discarding of parts or products fabricated with a deviation from the drawings or technology. The production process tests performed in the final operations make it possible to "clean" the batches of products manufactured with poor quality and assure the specified level of product quality. The more efficient the production process testing, the lesser the role of the output acceptance quality control.

The tests performed within the framework of input quality control of materials, semi-finished products, etc., are carried out in accordance with programs composed based on the technical specifications for their delivery.

All those tests which play a part in the technology in each operation and provide for checking the conformity of the product of a given operation to the requirements which are established are included among the production process tests performed in the process of fabricating the integrated circuits. Not just the indicated problem is solved by means of these tests. The scatter in the values of the major parameters of the IC's in the general set are reduced by means of them, the electrical characteristics are stabilized, by eliminating the causes of parameter drift with time, and what is the most important thing, the tests provide for sorting of the finished devices into groups as a function of their reliability.

Without going in detail into all of the tests included in operational quality control, we shall treat the latter in somewhat more detail, which we shall call quality control sorting.

Sorting tests, as the name itself says, pursues the goal of quality control sorting of all products into groups, depending on their quality. The necessity of these tests is due not only to economic considerations: the striving to extract the maximum income and make production profitable. An important factor which governs the expediency of incorporating sorting tests is the eternal lag of the production level of product manufacture behind consumer requirements. This especially concerns requirements placed on IC reliability. Here as nowhere else are the contradictions clearly manifest between the desire of the customer and the capabilities of production. The requirements on IC reliability and durability run ahead of the ability to achieve them, and even more to realize the requirements placed on the production process equipment, test facilities, methods and equipment for metrological support of IC production and checking IC quality, reliability and durability.

These tests are treated in detail in Chapter Five. For this reason, we shall limit ourselves here to a discussion of some procedural questions.

Rejection sorting test programs differ substantially from one another. The typical programs for such tests provided in U.S. military standard for semiconductor IC's MIL-STD-833 are presented in Table 15. They contain test operations and measures to artificially age the products, where these steps are called upon to ascertain defective and instable devices and to influence the remainder so that the causes of parameter drift are eliminated. Included among such measures are heat treatment of the IC's, which, as a rule, is carried out prior to sealing them and thermoelectric conditioning, which precedes the direct rejection sorting of the devices with respect to electrical parameters and specified reliability criteria.

Various deviations from the standard program are possible in different cases. The composition of the quality control, test and conditioning operations, their sequence, conditions and operating modes vary as a function of the purpose of the IC's, their structural design and production process features as well as the requirements placed on quality and reliability.

In all cases, the resolution of procedural questions of test conduct is governed by the following main principles:

--The choice of test types, methods and conditions should be based on knowledge of the physical essence of integrated circuit failures with exposure to various actions during their testing and operation, as well as on knowledge of their structural design and production process features;

--The test methods should accelerate the development of typical defects inherent in this IC design and given production process, but should not cause the appearance of new failure mechanisms not inherent in the given type of IC design and technology;

--The sequence for the performance of the tests should be chosen so that tests are performed first which provide for the greatest rejection of substandard products, and should contain the kinds of tests which make it possible to reject potentially unreliable integrated circuits.

TABLE 15. Program of Rejection Tests in Accordance with Method 5004 of MIL-STD-883

Kind of Test	Integrated Circuit Reliability Class		
	A	B	C
Visual inspection	Condition A	Condition B	Condition C
Artificial aging (stabilizing heat treatment)	24 hours	24 hours	24 hours
Thermal shock Thermal cycling	15 cycles 10 cycles	15 cycles or 10 cycles	15 cycles or 10 cycles
Mechanical shock	20,000 g	none	none
Centrifuging	30,000 g	30,000 g	20,000 g
Check of the hermetic seal	yes	yes	yes
Electrical tests	yes	no	no
Thermoelectric conditioning	168 + 72 hr	168 hr	--
Check of the electrical parameters	yes	yes	yes
X-ray flaw detection	yes	no	no
Visual inspection	yes	yes	yes

The effectiveness of quality control sortin tests is govern by the correctness of the choice of rejection criteria, the quality of the output product as well as the requirements placed on its reliability and the listing and conditions of the tests being performed.

It is not difficult to convince oneself of what has been said by glancing at Table 16, where figures are given which characterize the efficiency of rejection tests of IC's as a function of quality. As can be seen, the difference between the failure rate for various groups of integrated circuits reaches several orders of magnitude [32].

The governing factor when making a decision concerning the implementation of a particular program of rejection tests for the integrated circuits which are being produced is the economic factor. Tables 17 and 18, which were taken from the literature [23, 32], are convincing evidence in favor of this argument and show how great the losses can be if timely steps are not taken to reject units which do not meet definite requirements. The levels of reliability regulated by U.S. military standard MIL-STD-883 are presented in Table 17. The values of the IC failure rate, which represent the requirements of various users, are the requirements of three companies using the integrated circuits, reported to national symposia on reliability. The ARINC model is nothing more than the reliability

TABLE 16. The Effectiveness of Rejection Sorting Tests (Average Failure Rate per 1,000 hr, %)

(A) Качество партии (доля дефектных микросхем, %)	(B) Эффективность испытаний, %			
	0	80	90	99
1	0,02	0,004	0,002	0,0002
5	0,1	0,02	0,01	0,001
10	0,2	0,04	0,02	0,002

Key: A. Quality of the batch (fraction of defective integrated circuits in percent);
B. Test effectiveness, percent.

TABLE 17. Requirements Placed on Integrated Circuit Reliability as a Function of the Level of Complexity of Equipment Repair

Источник Source	(A) Интенсивность отказов за 1000 ч, %			
	Стандартные приборы Standard Devices	(B) Авиационные приборы (C) Ремонт осуществляется: легко Easily	трудно With Difficulty	(D) Космическая техника: ремонт невозможен или очень дорог
(E) Фирма TI	0,02—0,04	0,01—0,02	0,004—0,008	0,002—0,005
(F) Потребитель A	0,1	0,03	0,003	—
(G) Потребитель B	0,06	0,045	0,006	0,003
(H) Потребитель C	—	—	0,0038	—
(I) Модель ARINC	0,03	0,02	0,006	0,002
	(J) Относительная стоимость (индекс стоимости)			
	1	1,3	1,8	2,8

Key: A. Failure rate per 1,000 hr in %;
B. Aviation devices;
C. The repair is accomplished:;
D. Space equipment: repair impossible or very expensive;
E. Texas Instruments Company;
F. User A;
G. User B;
H. User C

Key [cont.]: I. ARINC model;
J. Relative cost (cost index).

standard computed from [106] which makes it possible to determine the indicator of product reliability improvement as a function of the kinds of rejection tests employed, the operational conditions and the position of the estimated value on the $\lambda = f(t)$ curve. The cost index is defined on the basis of the price of 100 TTL circuits with a low level of integration, sealed in C-DIP packages.

TABLE 18. The Cost of Class B Rejection Tests in Accordance with MIL-STD-883

Kind of Test	Cost, Dollars		
	Minimal	Average	Maximal
Visual inspection (condition B)	0.15	0.25	3.0
Heat treatment	0.01	0.05	0.10
Thermal cycling	0.05	0.10	0.20
Centrifuging	0.05	0.10	0.25
Check of the hermetic seal	0.05	0.10	0.20-0.25
Thermoelectric conditioning	0.25	0.50	5.00
Check of the electrical parameters	0.25	0.50	2.00
Total	0.81	1.60	10.55

However, it would be incorrect to evaluate only the economics. The decision to implement or not implement rejection tests should be made on the basis of the results of analyzing a set of questions, among which the main ones are the initial requirements placed on device quality, the permissible and justified degree of integrated circuit rejection at the level of modules and systems, the requirement placed on reliability and the degree of reproducibility of IC application conditions by standard programs.

The conditioning of integrated circuits, just as heat treatment, used for artificially accelerating the aging of IC's, is more of a production process operation than a test. In problems which are solved, for example, in the thermal and electrical conditioning of products, the functions of production process and quality control operations are interwoven, if a technological operation in this case is understood to be an operation called upon to generate definite quality properties in the product. It is not obligatory in all cases for all of the output products, but is used only when the issue is one of obtaining highly reliable products. The purpose of this operation can be formulated as follows: stabilization of product parameters, reducing the amount of drift in the major parameters of integrated circuits exposed to the applied load as well as the scatter in their parameters and the rejection of units which do not meet the set requirements.

The kind of conditioning is chosen by working from the definition we have given for it. As applied to electronics products, conditioning is the operation of the products in an electrical mode under definite environmental conditions. Specific features of semiconductor devices also do not preclude conditioning products in a de-energized state, but in an environment at an elevated temperature. For the sake of comparison we shall say: the conditioning of a bearing, crank mechanism or assemblies and products from machine building similar to them also consists in operating them, but the mechanical operation.

The aging conditions and modes are specified by working from the specific set task, the state of the product, its proposed quality and the requirements placed on the level of reliability. With the exception of individual cases, when one knowingly incurs any material expenses, the rule is the designation of aging conditions such that the cost of the conditioned integrated circuits does not exceed the cost of losses which can be incurred by integrated circuit failure during operation.

Quality Control Tests. Electrical Tests. In accordance with the standard of [101], electrical tests are those in which the main kind of exposure is to electrical loads.

Testing integrated circuits for non-failure operating time pursues the goal of evaluating their stability during and immunity to longterm exposure to an electrical load and an elevated temperature.

The tests are performed in a special chamber equipped so that is possible to place a considerable number of products under test in it at the same time and to create and maintain a temperature mode within a set precision for a long period of time while simultaneously applying an electrical load to all of the integrated circuits and monitoring the IC parameters without removing them from the chamber.

For the purpose of creating the worst case conditions for the products being tested, they are tested at the maximum permissible load in a static or dynamic mode.

In the static mode, either a reverse bias or forward bias voltage is fed to the IC's being tested. In this case, the integrated circuits operate at the ultimate permissible power dissipation.

The dynamic test mode is realized in one of the following variants: a parallel or series excitation circuit, or a ring oscillator circuit configuration.

In the first of these cases, the requisite supply voltages and the corresponding input signals are fed to the IC's under test, while the maximum load is connected to the integrated circuit outputs.

In the case of series excitation, the integrated circuits are connected in series: the output of the preceding one is connected to the input of the following one. The supply voltage is fed in, while an input signal is fed from an external generator to the input of the first IC in this circuit configuration.

Tests using a ring oscillator configuration differ from those treated above in that the requisite supply voltages fed to the products being tested, while the IC's are connected in series so that the output of the last one is connected to the input to the first.

Logic IC's are tested by any of the methods described here. As far as linear integrated circuits are concerned, they are tested using both variants in a static mode, while in a dynamic mode, they are tested only in a parallel excitation configuration.

The test procedure provides for placing the IC's in the test installation, checking the electrical parameters under normal climatic conditions, elevating the temperature in the working volume of the chamber up to the value corresponding to that indicated in the standard setting engineering documentation, and supplying the specified electrical conditions for the IC's.

During the testing process, the electrical parameters are monitored at definite time intervals. The list of parameters, the periodicity, as well as the techniques and equipment for the monitoring are indicated in the standard setting engineering documentation.

The tested integrated circuits, after being kept at normal conditions, are subjected to a final check: the external appearance and overall state are assessed visually, the parameters are measured and they are compared with the initial values. Those IC's are considered to have passed the test, the external appearance of which and the electrical parameters during and after the tests conform to the standards established by the standard setting engineering documentation. Durability tests are performed for the purpose of confirming the specified value of the minimal time before failure and the gamma percentage service life established in the standard setting engineering documents.

The tests are carried out under normal climatic conditions over a period of time no less than the minimum duration of the non-failure operating time. The electrical load is maximal. The circuit configuration is one of those treated above. The periodicity of the testing is specified by the standard setting document.

As result is considered to be a positive outcome when the external appearance of the integrated circuits and their electrical parameters conform to the norms of the technical specifications, of the testing program, and of the particular document which governs the rules and procedure for the conduct of the test.

The procedure for checking the durability of integrated circuits which is practiced in the majority of foreign countries provides for shipping the products ahead of schedule. The stimulus to work on improving the fabrication quality of IC's is expressed in the fact that for a specified test duration of 1,000 hours, the manufacturer gains the right to turn the product over ahead of schedule given the condition that 10 batches of the products tested sequentially for 500 hours showed a positive result. The conformity of the number of IC failures during the testing process to the acceptance number serves as a positive outcome for each test, while the criterion for the stability of the quality level of

the output product is 9 batches which have passed the testing out of the 10 subjected to the control testing.

Integrated circuits from a batch which did not pass the test undergo the complete program of quality control testing.

A high quality output product, which is characterized by the successful passing of 500-hour tests by 10 sequentially produced batches of integrated circuits gives the manufacturer the right to curtail the length of the tests to 250 hours. In turn, the success of such tests assures a further reduction in the testing time down to 100 hours.

Mechanical, Climatic and Biological Tests. The majority of the methods for mechanical, climatic and biological tests of integrated circuits do not fundamentally differ from the known methods of testing devices, equipment and their components. They have been covered sufficiently completely in the press [4, 104, 107-111], and we will not stop to describe them here.

We shall consider only those tests which are not used for quality control of devices and equipment and are employed only in integrated circuit testing. Along with this, we shall also analyze the so-called accelerated testing techniques.

Included among the group of tests to which only integrated circuits are subjected is a series of mechanical strength tests for the leads and connections: the testing of IC leads for bending and tensile strength, the testing of IC's for the strength of the joining of the chip to the substrate and testing the strength of the internal connections. Testing for lead wettability as well as IC testing for immunity to thermal shock, testing for the purpose of checking for the presence of an impermissible amount of moisture inside the IC package (dew point determination) and testing for immunity to exposure to dew are also included in this same group.

Bending tests of IC leads are performed for the purpose of checking the ability of integrated circuit leads, including their fastening assemblies, to stand up to a mechanical load applied perpendicularly or at some angle to the axis of the leads.

The test procedure consists in alternately hanging a load of a definite weight from each lead of the IC being tested. The integrated circuit is smoothly inclined over to an angle of 90 degrees. One bend contains the inclining and the return to the initial position. Several bending cycles are realized.

When testing for the purpose of evaluating the lead strength margin (in the standard setting engineering documentation, this test is frequently called a bending fatigue test of integrated circuit leads), the leads are bent through 90 degrees in both directions alternately. The bending radius and the point of load application are specified in the standard setting documentation.

A set of clamping devices and loads are used for the tests which assure the application of a bending load of a specified level to the leads of the packages

of the products under test. Moreover, a set of devices and attachments is used to prevent an end-restraint moment on the leads and to visually assess the results of the test. An outcome is considered to be a positive test result if there are no breaks in the leads or cracks in the insulators.

The resistance of integrated circuit leads to a load applied along the leads, i.e., to tensile forces, as well as the lead securing strength in this case are checked by applying a static load in the direction of the lead axis in a definite sequence to each lead of an IC. The size of the load is taken from the standard setting documentation as a function of the degree of severity established for the given product type. The time that the load is applied is figured in seconds. The procedure allows for leads which are directed coaxially opposite to each other to have a force applied to one of them while the other is secured. The result of tensile strength tests of IC leads is considered satisfactory if no breaks in the leads or cracks in the insulators are observed at the conclusion.

Methods are used for testing the strength of the internal connections in an IC which make it possible to determine quality of the seating of the chip on the substrate and the force needed to tear away the welded connections. In the first case, a load is applied by means of a special attachment to the chip uniformly over the surface area in a direction perpendicular to one of the side faces of the chip, so that the resulting force is directed at an angle of 15° to 20° to the surface of the substrate. The strength of the internal welded connections is checked by applying a load of definite size to the lead, which causes the contact connection or lead to break.

We shall conclude the treatment of mechanical tests with yet another curious circumstance in our opinion which undoubtedly deserves the attention of IC testers. It is asserted in [112] that in certain cases, tests using single shocks can be replaced by centrifuging.

When the necessity arises during tests with single shocks or in a centrifuge of providing for a pulse trapezoidal waveform with a rise time and leading edge decay figured in tens and hundreds of milliseconds, one of these types of load can be replaced by the other. The effect on the product under test proves to be equivalent in both cases if the width of the leading and trailing edges exceeds 0.09 seconds, while the law governing the rise and fall of the acceleration is linear. In this case, the run-up and shut-down time of the centrifuge is of no importance, and consequently, does not have to be standardized if the product being tested does not have components in it having a resonant frequency below 10 Hz. It is important to smoothly change the r.p.m.'s of the centrifuge. What has been said also applies to pulses of any waveform other than rectangular.

Besides the well-known widespread methods of checking product strength with exposure to mechanical shock, a fundamentally new method of quality control for connections is reported in paper [113].

The technique is based on a pulsed mechanical shock localized at a selected point, where the shock is produced by the energy due to the effect of electrical energy,

the pulses of which are delivered to the test object by an electron beam installation. The thermal energy occurring as a consequence of the breaking of the beam electrons in the material of the IC package, where the beam is produced by this installation, is converted to a compressive stress which acts on the IC leads in this case. The Febetron-705 installation designed for this purposed generates an electron beam with a diameter of about 25 mm having an energy of up to 2 MeV and directs it onto the test object in the form of a 30 nanosecond pulse.

Specialists of the Sandia Laboratories Company are proposing the use of this method for selective input quality control of the welding of tab leads.

The tests which determine IC strength with a sharp change in the ambient temperature and IC immunity to this type of effect are subdivided into thermal shock (heat shock) tests or thermal cycling testing. The essence of these tests is the same. The specific feature which distinguishes these tests, consists, first of all in the substantial difference in the time which is allocated for transferring the tested IC from an environment at one temperature to an environment at another temperature (during thermal cycling, this time is measure in tens of seconds, and when exposed to thermal shock, it is measured in seconds), and secondly, by the nature of the test environment (thermal cycling is done in air and thermal shock testing uses a fluid).

The integrated circuits being tested are placed by turns in the test environment, having a particular ultimate temperature, and are held there for a period of time indicated in the standard setting engineering documentation.

For convenience, the IC's are placed in special container plates, which provide for direct contact of the products being tested with the test medium.

Liquid nitrogen, a mixture of alcohol and dry ice, ice and glycerine are used as such a medium. The choice of the material for creating the environment is governed by the specified temperature. A "deep" cold is achieved using liquid nitrogen, a temperature of zero is reached by means of using thawing ice, and a temperature intermediate between them is achieved with a mixture of alcohol and dry ice. A positive temperature is achieved using glycerine. Various brands of glycerine are used, depending on the specified temperature.

The temperature limits, the duration of the exposure of the tested products to the test conditions and the transfer time, number of cycles and parameters being monitored are stipulated in the standard setting engineering documentation.

The tests are performed in special baths or chambers, which provide for the stable maintenance of a specified test medium temperature.

The integrated circuits which pass these tests, after being kept under normal climatic conditions, are subjected to visual and electrical testing and checked for hermetic seal integrity. Those IC's which are considered to have passed the test are the ones which meet the requirements of the standard setting engineering documentation with respect to all criteria.

The determination of the dew point is accomplished for the purpose of establishing the possibility of the appearance of moisture inside an IC package in such a quantity that it leads to an impermissible change in the electrical parameters of the IC when the ambient temperature changes.

Integrated circuits are tested in a thermal chamber, the temperature in which exceeds the ambient temperature by an average of 10° C prior to the start of the test. Having measured the parameters of the IC under test, the electrical load is not removed. The parameters are monitored during the testing.

The test consists in changing the temperature in the working volume of the chamber from positive to negative and again to the former positive value at a certain rate. The duration of the temperature change from one ultimate value to the other depends on the range of temperature change and is figured in minutes. A change in IC parameters within permissible limits, stipulated in the standard setting engineering documentation, attests to IC capability of maintaining operability under conditions of an unavoidable dewfall.

A variant of this test is the checking of the ability of IC to operate in the presence of frost. The procedure provides for the coating of the IC with frost and its subsequent thawing. To reproduce the test conditions, the integrated circuits which are tested for conformity to the requirements of the standard setting documentation with respect to the main electrical parameters, are kept for several hours at a slightly negative temperature (20 - 30° C) [sic]. After this, they are removed from the chamber and kept for several hours under normal conditions in an energized state. The electrical parameters are checked periodically. The conformity of these parameters to the requirements of the standard setting documentation serves as the criterion for positive outcome of the check of the given quality property of the unit being tested.

IC testing for moisture immunity, performed in a cyclical variant, is included among the number of accelerated testing methods.

Thermal cycling makes it possible to speed up the process of microdefect development in the package protection for an IC, on the surface, in the internal circuit wiring layout and other areas, which in a medium with elevated humidity can lead to a considerable change in the parameters.

The graphs in Figure 28 (a-c) illustrate the changes in the test mode parameters over the course of one cycle. As follows from these graphs, the tests are performed primarily in a heat and moisture chamber, where the temperature is changed cyclically from the normal value to the working and ultimate temperatures for the given type of IC's [107,109].

Each test cycle consists of exposing the integrated circuits to an atmosphere with an elevated humidity at an elevated temperature and subsequently changing the temperature while maintaining the relative humidity constant. The ratio of the duration of the exposure and the period of temperature change depends on the design of the product and the problem being solved. It is usually chosen in a range of from 1:1 to 1:0.17.

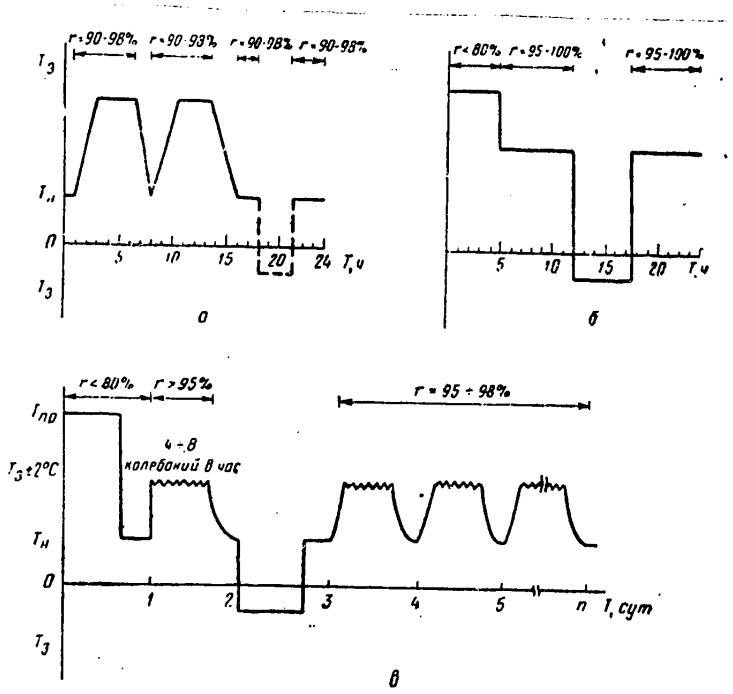

Figure 28 (a-c). Schematic of a single test cycle for moisture immunity according to various standard setting engineering documents.

Key: 1. Four to eight fluctuations per hour.

A typical test procedure provides for the preliminary exposure of the IC's to an elevated temperature and normal humidity for several hours. After this, the temperature in the chamber is reduced down to normal and the electrical parameters are checked.

Following this, a humid environment is created in the chamber, while the temperature is periodically varied in a specified range.

Besides the steps described here, this kind of testing procedure provides for exposing the IC's to a below freezing ambient temperature or vibrating them with subsequent checking in a humid environment as the concluding step. The requisite effect is achieved by combining the steps and changing their sequence and duration.

The rate of temperature change is usually not standardized.

The quantity of air which is fed into the chamber every minute should exceed the chamber volume by a factor of no less than five times.

The vibration of the integrated circuits is realized in the low frequency range (10 to 60 Hz) with a continuous frequency change from the lower ultimate value to the upper value, taking an average of 1.5 minutes.

At the end of the concluding cycle, the IC is exposed to an environment with elevated humidity and a normal temperature.

Chemical Tests. Solder wettability tests of integrated circuits leads pursue the goal of checking the preparedness of the leads to take solder. The second problem which is resolved in this case is an additional check of the thermal immunity of the IC during the soldering of the leads. Since touching a heated soldering iron to an IC lead is accompanied by instantaneous local heating, the capability of the IC to stand up to the effect of a thermal shock is checked.

The testing procedure provides for degreasing the leads with alcohol and subsequent treatment with flux. Then the wettability of the IC leads with solder is to be checked. It is accomplished by immersing the free ends of the leads in solder, having a temperature which is stipulated in the standard setting engineering documentation. The duration of one testing cycle is governed by the testing documentation and amounts to several seconds. The solder should conform to definite specifications. The major one of them is a clean and shiny surface of the melted metal.

Sometimes the testing is complicated. In these cases, prior to treating with flux, the degreased leads are exposed for several tens of minutes to distilled water vapor.

The IC under test is suspended above the surface of boiling water at a distance such that the ambient temperature does not exceed the value of the working temperature of this type of integrated circuit. The integrated circuit is exposed for several hours to normal climatic conditions between the above indicated operation and the testing.

The thermal immunity of an IC during soldering is checked by repeated immersion in solder with an interval between the sequential immersions lasting no more than five minutes. The temperature of the solder in this case is elevated an average of 20° C with respect to the temperature of the solder when testing for lead wettability.

A tin bath equipped with a heat regulator is used for the testing and provides for a stably maintained specified temperature. Moreover, equipment is used which provides for convenient and reliable immersion of the IC leads in the solder to the requisite depth. To be numbered among the other equipment needed for this test are the tank for checking the IC immunity to thermal shock during soldering, an optical instrument with a magnification of 16 x and instrumentation for monitoring the integrated circuit parameters.

Visual inspection of the IC's following solder wettability testing of the leads should establish the absence of cracks on the surface of the leads as well as corrosion pitting, bared sections and bubbles.

The assessment of the test results using optical equipment with a magnification of 16x should show the absence of peeling, layer separation or bubbles in the coating during bending of the leads through 180°. The IC leads are bent in a radius equal to half of the lead diameter. Integrated circuits, in the leads of which cracks are found in the metal coatings or traces of corrosion are rejected.

A positive result is considered to be such a test outcome that the surface of each of the tested IC is coated with a solid layer of solder over no less than 95%. In this case, its individual punctures and cavities are scattered over the entire surface, and not concentrated at one point, there is no mechanical damage and the electrical parameters conform to the requirements established in the standard setting engineering documentation.

Hydrolic (Pneumatic) Tests

In accordance with the classification given in the literature [101], to be included among this group of tests are IC tests which pursue the goal of evaluating the hermetic seal of the package protection. These tests are based on the recording of the gas exiting through a hole in the product package, by means of a special leakage indicator or visually.

In the standard [101], tests in which the major kind of exposure is to fluid or gas pressure are called hydrolic and pneumatic tests. One can agree with such a classification with certain conditions, however, the detailed definition of these tests shows that it is nonetheless closer to reality to include them among the group of climatic tests.

Apparently, it would be correct to additionally introduce into the standard of [101] yet another classification group of tests: hydrolic tests, and to include in it all kinds of tests related to checking the hermetic seal of the package protection for integrated circuits and other products, as well as to the estimation of the water, spray and droplet immunity of the components and assemblies of instruments and equipment.

Minor defects in the package protection of integrated circuits which are responsible for a complete hermetic seal in the range of "small" leaks are determined by mass spectrometry. The integrated circuit or batch of integrated circuits are pressurized with helium, and then the rate of helium leakage from the IC package is checked. A special pressurization chamber is used for the pressurization. The pressurization is accomplished at a pressure exceeding five atm, for a period of time of no less than three hours. With a lower pressurization pressure, its duration is increased. Having completed the pressurization, the pressure in the chamber is reduced to normal and the units are transferred to a control chamber, where the rate of gas leakage is measured based on the expiration of a definite time (up to one hour).

Used for the tests are an integrated circuit pressurization chamber, a mass spectrometer for monitoring the hermetic seal with a leakage indicator, having a sensitivity sufficient to register a helium leakage rate of no worse than 10^{-7} $l \cdot \mu m/sec$; a diffusion type leakage reference standard and a production process case for storing and transferring the integrated circuits.

Integrated circuits, the leakage rate of which does not exceed that set by the standard setting documentation are considered to have passed the test.

The techniques provides for the determination of the hermetic seal in a range of from $1 \cdot 10^{-3}$ to $1 \cdot 10^{-7}$ $l \cdot \mu m/sec$. In using this method, it is essential to observe that all of the plug connections have a vacuum seal within the sensitivity range of the leak sensor, while the leak sensor is graduated in accordance with a standard diffusion type leak.

So-called "moderate leaks", i.e., defects due to a hermetic seal failure which is characterized by a value of $1 \cdot 10^{-2}$ $l \cdot \mu m/sec$ and more, are determined visually based on the leaking of gas out of the IC package.

The IC's are pressurized with freon in a chamber where the ambient pressure is brought down to 1 mm Hg. The freon is fed into the chamber at a pressure of 3 to 5 atm. The duration of the pressurization usually runs to three hours and more. Following the indicated exposure of the units being tested to the freon, the pressure is reduced down to the normal level, and the IC's are dried and transferred to a bath with heated ethylene glycol or another fluid with similar physical properties. The presence or absence of gas bubbles exiting the IC package at points where there is a seal failure is detected visually. The absence of bubbles attests to the hermetic seal of the package. IC's are tested in an indicating fluid with the cap down. The depth of immersion of the products in the fluid should be such that the bottom of the IC package is no less than 50 mm from the surface of the liquid. The temperature of the liquid is specified in the standard setting engineering documentation.

The result of the testing is observed and recorded for 10 to 30 seconds. If several IC's are subjected to testing at the same time, it necessary to arrange them so that the appearance of individual bubbles at each of them will not go unnoticed by the observer and will be immediately registered.

To test the hermetic seal of integrated circuits with this method, it is necessary to have a pressurization chamber: a high pressure vessel, a transparent bath with a grid of stainless steel at a spacing of 50 mm and more from the bottom of the bath, freon, ethylene glycol or another fluid suitable for indication purposes, a magnifier for observing bubbles and a thermal regulator which maintains the liquid temperature in the bath in a range of $\pm$ 3° C.

An IC seal failure estimated to have a leak exceeding 1 $l \cdot \mu m/sec$, is monitored, just as in the case just described here, but without preliminary pressurization. The dimensions of defects which determine the seal failure of a product package are such in this case that there is no need for pressurizing the package. Integrated circuits with seal failures placed in ethylene glycol, glycerine or another indicator fluid give off bubbles.

The procedure for performing the test provides for heating the indicator fluid up to a definite temperature specified in the standard setting documentation. The tested samples, just as in the case already considered here, are immersed in the indicator fluid to a depth of no less than 50 mm from the surface of the fluid.

The same equipment is used for the testing as when checking "moderate" leaks.

The gas inside the IC package expands and gets out through the holes, forming bubbles.

Besides those considered in worldwide practice, other methods are also used for checking the hermetic seal of IC packages.

Cyclical tests for moisture immunity are successfully employed to ascertain large and moderate leaks. Defective integrated circuits are detected from the departure of the parameters from the norms because of the increase in the leakage current and the reduction in the inverse breakdown voltage and gain of the transistors.

The use of dyes makes it possible to precisely locate a seal failure point. When checking the hermetic seal of IC packages to detect leaks through cracks in the glass or defects in the seal of the pins to the glass, luminescent monitoring is frequently used. It consists in making the leaks visible with ultraviolet light.

In conclusion, we shall deal with yet another method of checking a hermetic seal, which some investigators include among accelerated techniques. The issue involves testing integrated circuits under pressure in an aqueous solution of substances which have a strong influence on the state of the surface of the semiconductor chip. The sensitivity of the method is higher than some others. However, the use of this methods entails a danger of the gradual failure of the IC being checked, if it has been acknowledged as a good one initially. A portion of the solution, having entered into capillary holes during the testing, will move during an extremely long period of time into the interior cavity of the package, and having penetrated there, can unexpectedly cause the device to fail.

Nondestructive Integrated Circuit Quality Control Methods. Nondestructive methods are becoming increasingly widespread among the various techniques of IC quality control testing. Their widescale introduction into quality control practice is explained both by technical and economic considerations.

Quality control which is accomplished using nondestructive techniques makes it possible to operationally timely determine the properties and state of the raw materials and finished products, without rendering them unsuitable and without reducing their operability and service life. The techniques are highly productive and economical. They provide for an individual check of the quality of manufactured IC's and the apriori evaluation of their reliability. These methods are finding ever greater applications not only for quality control, but also for failure analysis for the purpose of predicting the reliability and durability of integrated circuits.

Without going into the fine points of the classification of the numerous techniques of nondestructive testing, we shall briefly treat those which have recommended themselves as the most efficient as applied to integrated circuits [138, 125, 126].

Optical (Light) Microscopy. Modern optical microscopes (general purpose, metallographic, biological, comparison microscopes, etc.) are extremely sophisticated tools for quality control and research, having definite advantages over the scanning electron microscope: the color image, the simplicity of use, the possibility of directly observing the units being studied (tested), and the wide range of optical radiation properties which can be utilized (interference, polarization, luminescence, optical spectral properties of the radiation, etc.).

Optical microscopes make it possible to observe microscopic objects in a wide range of magnifications (from 3x up to about 1,800x) with a resolution of approximately 0.2 μm.

In this case, plates and finished IC's with such microdefects as mechanical damage and disruptions of the topology (size, mutual position, etc.) of individual structure components, contamination and chemical destruction of IC components (thin film conductors and resistors, dielectric coatings, wire leads, package components, etc.) are efficiently detected.

Interferometry Techniques. An important variant of the optical microscopy method is interferometric techniques based on the observation of the distribution pattern of the intensity and phase of optical radiation from a microscopic object when it is illuminated by a monochromatic incoherent or coherent source.

When observing the interference pattern from a flat plate in a microinterferometer, for example, from oxidized silicon, parallel lines are visible (interference maxima), which are positioned at an equal spacing from each other; in this case, the pattern does not change with an increase or decrease in the optical path difference by an amount equal to a whole number of half-wavelengths ($\lambda/2$) of the incident light. The presence of microinhomogeneities in the relief of the surface being studied (or local sections of transparent coatings with different indices of refraction) leads to the curvature of the bands. Measuring the amount of the curvature and comparing it with the spacing between adjacent parallel interference lines and with the quantity equivalent to half of the incident light wavelength makes it possible to determine the size of the relief unevenness (or the inhomogeneity of the optical properties of the transparent coating).

Optical interferometry makes it possible to measure relief steps in an opaque substrate of down to 0.1 times the spacing between the interference maxima, i.e., the resolving power of the technique is about 0.03 μm.

Infrared (IR) interferometry is based on the use of the monochromatic IR beam of a laser instead of visible light, which makes it possible to check plates of a semiconductor material of different thicknesses, observing and measuring the interference pattern by means of an electronic optical converter or a vidicon, sensitive in the IR region [114]. Thus, for example, for measurements at a wavelength of 1.15 μm, the index of refraction of silicon for which is 3.4, the spacings between the interference maxima are equal to $\Delta = 1.15/(2 \cdot 3.4) = 0.17$ μm. Assuming a measurement precision in this case of $(1/5)\Delta$, we determine the resolving power of the technique to be about 0.03 μm.

Ellipsometry. The ellipsometry method is based on the change in the parameters of elliptically polarized light as a result of its reflection from the object being studied.

The appearance of lasers which make it possible to obtain narrow, nondiverging monchromatic beams of light at a high intensity, have made it possible to use ellipsometric techniques to study the regions of thin films of oxide and nitride layers on reflecting surfaces [114]. In this case, measurements can be made in small dimensional ranges (10^{-5} to 10^{-6} cm^2), having thickness inhomogeneities on the order of a few tens of Angstroms, which is 5 to 10 times greater than the capabilities of optical interferometry. Using this technique, one can effectively monitor the quality of opening windows in silicon oxide or nitride during photolithography, determine plates which have been poorly cleaned, the thickness of the oxide and foreign films on which can amount to 4 to 5 nm (the thickness of the natural oxide on semiconductor plates usually does not exceed 2 to 3 nm); monitor the processing quality (cleaning) of the glasses used in the fabrication of the photographic templates; study the changes in the index of refraction of oxide, nitride and other transparent thin films, etc.

Optical Scanning Microscopy. One of the effective techniques of ascertaining defects and studying the failure mechanisms of integrated circuits, related to processes on the surface of a passivated structure, is the technique of semiconductor structure light response [115, 116].

The basis for this method is the measurement of the photoelectric e.m.f., which occurs when a semiconductor structure is illuminated with an intense light beam (probe). Since the level of the light response signal depends on the electrophysical properties of the semiconductor material, the p-n junctions and the properties of the semiconductor chip surface, the recording of local light response signals from various points in the structure being studied makes it possible to ascertain and study IC defects.

The physical principle of the operation of a scanning optical microscope is based on generating minority current carriers in the semiconductor with the action of light radiation. The charge carrier pairs generated by the light, in propagating in all directions from the point of generation by virtue of diffusion, reach the p-n junction and are separated by its field. In this case, a photoelectric e.m.f. appears across the p-n junction which causes a current to flow when the p-n junction circuit is closed.

When a chip is illuminated with a localized light beam, the photoelectric current will depend substantially on the point of beam impact. If the distance from the point of impact to the p-n junction is large, the photoelectric current is vanishingly small, since the nonequilibrium electrons and holes have time to almost completely recombine, before reaching the junction. If the beam falls in the space charge region of a junction, then all of the generated carriers participate in producing the photocurrent. When the light spot falls on a thin film metal conductor, the photocurrent disappears. If there is an opening (defect) in the metal film, the photocurrent rises. If there is a localized inversion layer

close to the p-n junction, the photoelectric current will not fall off over the entire extent of the junction, because of the inversion layer. When a portion of a p-n junction is illuminated in which there is an accumulation layer, the current carriers generated by the light cause avalanche ionization, leading to a sharp increase in the light response signals.

An optical scanning microscope takes the form of an installation with electronic scanning of the light probe and the use of scanning to obtain the light response images. The light source in it is a projection electron gun tube, while the light response image is produced on the screen of a television display tube with synchronized sweep.

As an example, we shall indicate the major technical characteristics of the domestically produced "Fotoskan" scanning optical microscope [115]:

Resolution	down to 2 μm
Magnification	30 to 300x
Field of view	from 0.2 x 0.2 to 5 x 5 mm^2
Light spot scanning rate	10 and 2 m/sec
Frame frequency	12.5 Hz
Number of lines in a frame	270
Weight	30 kg
Overall dimensions	1,300 x 600 x 400 mm

It follows from what has been said above that the major advantage of a scanning optical microscope is the capability of simple and rapid detection of bipolar and MOS integrated circuits with "inversion channel", "microplasma breakdown of the p-n junction", "metallization damage", etc. type defects. An additional advantage of a scanning optical microscope over a scanning electron microscope, with which one can also identify inversion channels (in an induced current mode) is the complete reproducibility of the results, since a scanning optical microscope does not lead to the degradation of the surface properties.

Laser Scanning Microscopy. A variant of scanning optical microscopy is the laser scanning technique [116].

A helium-neon laser with power level of 4 mW generates a beam, which is focused by a special device into a spot with a diameter of 1 to 2 μm. The scanning along the x axis is accomplished at a frequency of 600 Hz and along the y axis in a range of 1 to 10 Hz. Moving along the surface of a chip, the beam produces changes in the chip conductivity, which cause a change in the current passing through the chip. An image of the chip surface appears on the screen of a television set, synchronized to the laser beam scanning system.

Scanning the surface of an IC with a laser beam makes it possible to ascertain breaks in the metallization as well as various defects in resistors and diodes in an operationally timely manner and without difficulty. The concentration of the doping impurities, and consequently, the resistance of the resistors can be measured with it. Under the appropriate conditions, by using a laser beam to

generate a base current, one can turn on or saturate the transistors of IC's and thereby check the correctness of the performance of various logic operations by definite functional assemblies of an integrated circuit.

The proposition has been advanced [116] that in the immediate future, it will be possible to introduce the system on a production line, and after a while, by employing a modification of the given system using computers, one will be able to create a fully automated production line for integrated circuits.

The use of this method in the early stages of IC fabrication will assure the timely, inexpensive and more efficient rejection of defective integrated circuits.

Testing Methods Using Electron and Ion Microprobes. A substantial drawback to electrophysical and optical testing techniques is the fact that they basically provide information on the spatial inhomogeneity of microscopic objects and only indirect information on the inhomogeneity of their composition.

For effective checking of the inhomogeneity in the composition of materials, which provides for the localization necessary for the purpose of microelectronics, methods are employed using electron or ion beams with energies on the order of tens of kiloelectron volts, focused in a fine beam (a probe) [117]. Extensive information can be obtained on microscopic objects by means of measurement facilities designed around electron and ion probe excitation of solids with various recording techniques (electron and ion microscopes, X-ray microscopic analyzers, installations for observing cathode luminescence spectra, etc.). The schematic shown in Figure 29 illustrates observation possibilities using an electron probe microanalyzer.

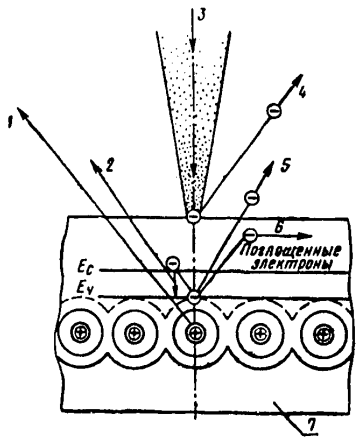

Figure 29. Symbolic representation of the major physical phenomena which accompany the interaction of electrons with solid matter.

Key: 1. X-ray radiation;
2. Cathodoluminescence;
3. Primary electrons;
4. Reflected electrons;
5. Secondary electrons;
6. Absorbed electrons;
7. The solid

Local X-ray spectrum analysis is an extremely promising means of checking the inhomogeneity of the composition of semiconductor materials.

This method is based on the spectral analysis of the characteristic radiation excited in local sections of the test object when it is bombarded with an electron beam having electron energies on the order of several tens of KeV by virtue of rearranging the inner electron shells of the excited atoms of the material. By determining the intensity of the spectral lines of the elements included in the composition of the object being studied, a qualitative and quantitative analysis can be made of the composition of the material.

The method makes it possible to confidently identify the elements of Mendeleyev's periodic table from sodium to uranium. The surface localization which is provided by the local X-ray analysis with a probe size on the order of one μm usually amounts to 2 to 5 μm. The relative sensitivity of the method, as a rule, does not exceed 0.01 to 0.1% by weight (10^{18} - 10^{19} atom/cm^3); the error is no more than 2%.

Microcathodoluminescent analysis successfully complements local X-ray spectrum analysis as applied to semiconductors with "forward" junctions, making it possible to eliminate the major drawbacks to the latter: the comparatively poor relative sensitivity, and the difficulty of identifying light atoms which have long wave radiation.

This is achieved by simultaneously recording the optical radiation in the electron probe microscopic analyzer with the X-ray radiation (see Figure 29), something which is accomplished by means of an optical spectrometer when the material is bombarded with an electron beam having electron energies of a few electron-volts.

Microcathodoluminescent analysis has significantly greater sensitivity (10^{16} atom/cm^3 and lower when the samples being studied are cooled) as compared to local X-ray analysis, something which is explained by the absence of phenomena similar to X-ray bremsstrahlung in the case of cathodoluminescence.

This method makes it possible to analyze the composition of thin films with a sufficiently high precision (for example, those based on gallium arsenide). In this case, the size of the error even for light atoms does not as a rule exceed 1%, while the surface locality amounts to 5 to 10 μm.

Unfortunately, the method is inapplicable to the testing of silicon, which has a low probability of radiative recombination.

Auger Analysis. The measurement of the energy spectrum of secondary electrons (see Figure 29), which fly out from a sample when it is bombarded with an electron beam having an energy of several KeV, can be used to detect light elements [113, 118]. In this case, only electrons which exit from the surface are suitable for the analysis, since their energy is not lost in collisions.

This method has a high sensitivity, making it possible to detect impurities with a concentration of down to 10^{18} atom/cm^3 at a depth of from 1 to 2 nm with a resolution of 20 to 50 μm, where it can be used to study silicon plates.

Ion Microanalysis. The techniques of local X-ray spectrum and microcathodoluminescent analysis are not suitable for checking the composition of semiconductor layers with a thickness on the order of several hundreds or thousands of Angstroms, since their localization cannot be less than several microns because of the diffusion scattering of the electrons. The distribution of the atoms of the material in such layers can be tested by means of ion microanalysis.

A beam of primary ions, for example, argon or oxygen (beam diameter of from 50 μm up to 1 mm and a primary ion energy of up to 15 KeV) is directed from an ion gun onto the sample being studied. In this case, the ion gun can be focused down to 2 μm [119].

In the case of ion bombardment of a test object, secondary ion-ion emission occurs as well as cathode sputtering, ion-electron emission and electromagnetic radiation.

Ion microanalysis is based on the phenomenon of secondary ion-ion emission. The secondary ions are directed to a mass analyzer by means of an immersion lens and following the appropriate filtering, fall on the cathode of an ion-electron converter, where the ion-electron emission occurs. The accelerated electron flux is deflected by a magnet to a scintillator, from which the light signal is fed either to a photomultiplier or to the ocular of a microscope.

It is more expedient to use an ion microanalyzer to identify inclusions in thin layers (of up to a nm) of semiconductor materials containing the lightest atoms (for example, hydrogen, lithium, beryllium, boron).

The sensitivity of an ion microanalyzer differs substantially for the various elements, however, it is significantly higher than the sensitivity of the two techniques indicated above and can reach 10^{11} - 10^{15} atom/cm^3, which is not the limit either.

It should be noted that ion bombardment destroys the surface, i.e., this technique cannot be included among nondestructive methods, however, it makes it possible to determine the distribution of doping impurities with respect to depth in a thin semiconductor layer relatively rapidly with a sensitivity inaccessible to any other technique, and from this point of view, is a powerful tool for the physical technical analysis of microelectronic devices.

Scanning Electron Microscopy. A scanning electron microscope is most frequently used as an effective means of studying microscopic objects, which include, in particular, integrated circuits.

A large number of different models of scanning electron microscopes are used for research purposes, however, their operational principle is similar [120-122].

The major part of the microscope is the vacuum chamber in which the electron gun and the magnetic focusing and deflecting lenses are placed. The electron beam emitted by the gun is focused by the lenses down to a diameter on the order of 0.2 μm and impinges on the sample being studied. The deflecting coils which accomplish the scanning provide for obtaining a raster sweep over the surface of the sample. In this case, the coils which accomplish the scanning are controlled by a generator which simultaneously controls the beam sweep on the screen of a cathode ray tube. Thus, the scanning of the CRT beam is accomplished synchronously with the scanning of the sample being studied.

The various methods of electron scanning microscopy are classified as a function of the kind of physical phenomenon employed, which accompanies the interaction of the primary electron beam impinging on the surface of the sample being studied with the material of the latter (see Figure 29). A brief description of the characteristics of electron microscopy techniques using this principle, with an

TABLE 19. Methods of Scanning Electron Microscopy and Their Applications to Microelectronics

Designation of the Method	Kind of Physical Phenomenon Employed, which Accompanies the Interaction of Electrons with the Material Being Studied	Area of Application of the Method in Microelectronics
1. The reflected electron technique	Elastically and inelastically reflected primary electrons	Microtopography of an IC (quality of the metallization, steps in relief, quality of the oxide, welded contacts, surface contamination, etc.)
2. The secondary electron emission technique	Secondary electrons emitted from the material as a result of secondary electron emission	Integrity of electrical circuits, determination of the electrical potentials of individual elements
3. The absorbed electron technique	The electron current from electrons absorbed by the material	The same
4. Cathodoluminescence (microcathodoluminescent analysis)	Emission of electromagnetic radiation in the visible or infrared portion of the spectrum	Identification of inhomogeneities in the concentration of the doping impurities. Determination of crystalline structure defects
5. The technique of transiting electrons	Primary beam electrons which pass through the material	The same
6. X-ray microanalysis (local X-ray spectrum analysis)	Characteristic X-ray emission of individual chemical elements	Chemical composition of the material and local inhomogeneities in the layer near the surface of a semiconductor, and thin film elements. Identification of contaminants
7. The induced e.m.f. technique	Induced e.m.f. occurring in a product because of the separation of electron-hole pairs by the p-n junction, where these pairs are generated by the electron beam.	Identification of inversion channels, surface structural defects, local regions of microplasma breakdowns, and the temperature distribution of some elements

TABLE 19. [cont.]

8. Scanning reflected electron microscopy	Electrons reflected from an equipotential surface located in the immediate vicinity over an electrically energized product	The identification of inversion channels, surface structural defects, local regions of microplasma breakdowns and the temperature distribution of certain elements

indication of their areas of application for purposes of studying integrated circuits, is given in Table 19 [113, 117]. A portion of these methods has already been treated above (local X-ray spectral analysis, microcathodoluminescent analysis). In this section, we shall briefly deal with the capabilities of reflected electron techniques as well as secondary electron emission and induced e.m.f. methods, which are finding increasingly greater applications in microelectronics. The major advantages of a scanning electron microscope over an optical microscope consist in the large range of magnification (5 to 50,000x), the high resolution (15 to 20 nm) and the great depth of definition, as well as operation in a wide range of modes, which make it possible to gather extensive information on the characteristics of the object being studied.

Thus, for example, by using a scanning electron microscope in a reflected electron mode, one can obtain a high quality magnified image of any portion of an integrated circuit on the screen and record it on photographic film. The magnification factor varies in this case in a very wide range.

A precise quantitative evaluation of the results of measuring surface relief is possible by means of stereophotography.

In a scanning microscope, the stereophotography is accomplished by obtaining two photographs of the section under study at different angles. For this, the integrated circuit is positioned strictly in the center of the frame. The resulting stereo pair is treated by means of a mirror-lens stereoscope, which makes it possible to identify the desired point in any of the photographs. A stereoscope which provides for the measurement of a vertical relief component with an error of no more than 5% is suitable for such applications.

In order to illustrate the capabilities of a scanning electron microscope, we shall describe the operations in analyzing an IC which has failed, which can be sequentially carried out without removing the IC under analysis from the vacuum chamber of the microscope.

Having discovered the defective element of the IC (a thin place in a thin film conductor, damage to a wire lead, contamination of the surface or a change in

the color of the metal or oxide because of the presence of an inclusion of unknown origin, etc.), one can measure the geometric dimensions of the elements, or having connected an accessory for X-ray microanalysis, use the scanning electron microscope for the operationally timely identification of the chemical composition of the unknown material. Having made electrical contacts beforehand to the sample being studied, one can study it in a secondary electron emission mode or using the induced e.m.f. technique without extracting the integrated circuit from the vacuum chamber, and determine whether the just detected contamination is the reason for the inversion or ion type leak, or whether it is the cause of the chemical destruction of a thin film conductor, resistor, etc. All of this increases the effectiveness of physical and technical analysis to an extraordinary extent when determining the kind, cause and source of a failure.

Moreover, in a number of foreign companies - IC manufacturers, scanning electron microscopes are used in IC production to optimize the production process modes and selective quality control, for example, for thin film conductors (especially when fabricating large scale integrated circuits with multilevel interconnections) [113].

Equipment complexity and expensiveness, as well as the difficulty of interpreting the resulting information in a number of cases and the changing of the surface properties of an IC (for example, the induction of a positive charge with the action of high energy electron beams), which can lead to distortion of the data, and in a number of cases, to irreversible changes in the characteristics of the sample being studied, must be included among the drawbacks to scanning electron microscopy techniques.

However, these drawbacks to the methods of scanning electron microscopy are completely compensated for by its numerous advantages, which makes the given group of techniques an irreplaceable tool for the study and testing of integrated circuits, especially large scale integrated circuits which are characterized by considerable functional complexity.

Thermal Infrared Analysis. Of the numerous techniques for the thermal investigation of electronic equipment products (temperature field and thermal radiation field methods) in microelectronics, the most intensive efforts are under way in using the passive infrared technique with various ways of recording the IR radiation of an IC chip, the heating of which is caused by the current flowing under various electrical operating conditions of the IC.

Studies demonstrate that the isotherm of the maximum temperatures pass through regions where the p-n junctions, resistances and defects are located, which lead to local overheating of the IC components.

Infrared radiometers are microscopes which are equipped with detectors for the IR radiation emitted by an operating integrated circuit. Series produced models of foreign IR radiometers have a temperature range of from 25° C up to 400° C, a sensitivity of 0.5 to 1° C and a "spatial" resolution on the order of 10 to 20 μm [113].

One of the major difficulties inherent in this method is related to the difference in the emissivity of materials, because of which the intensity of the IR radiation emitted by two different materials (for example, aluminum and silicon dioxide) at the same temperature is not the same.

Coatings with an identital thermal emissivity can be applied to devices, however, this solution is obviously not an optimal one, since the coating itself can have an impact on IC operation.

This problem can in principle be solved through the use of computer methods of processing the data obtained when converting the thermal radiation fielf to the true temperature of the IC elements.

The design of a TV microscope is reported in [123], which makes it possible to find the localized sites of excess heat in high power IC's. The IC is placed beneath the microscope objective with a magnification of 125x, and its thermal profile is observed on the screen. All of the changes in the observed picture which are due to a change in the electrical conditions are noted visually by the controller. The device makes it possible to study thermal fields with a size of down to 0.6 x 0.6 mm. The minimum temperature difference is 0.6° C.

X-ray Techniques. In addition to the methods of nondestructive testing treated above, X-ray diffraction analysis is being successfully used to ascertain hidden production defects in finished integrated circuits. The method is based on the comparison of the X-ray diffraction patterns of the IC being studied with a "reference standard" X-ray pattern, in which integrated circuits having typical s are depicted.

X-ray diffraction analysis is accomplished by means of an X-ray machine with a voltage range of up to 150 KV and a focal spot of no more than 1.5 mm. The films are interpreted using any suitable device. In particular, the 5PO-1 microfilm reader is used for this purpose.

The quality of the cap seal to the IC package, the quality of the internal interconnections, the plate or the glass as well as the absence of foreign particles in the device package are checked with the X-ray technique.

When it is not necessary to document the results of the quality control check, X-ray television is used to check the quality of IC's. With this method, an X-ray image converter and a closed television system, which make it possible to visualize the X-ray image, are used to record the shadow X-ray image.

In the case of X-ray television monitoring [124], X-ray TV's are used, which have a resolution of 20 to 100 pairs of lines per mm, a contrast sensitivity of no worse than 5% and a magnification of from 20x up to 200x.

Work on nondestructive methods of ascertaining the hermetic seal integrity of packages has been widely implemented in practice. Along with those considered above, these techniques provide for the rejection of defective and potentially unreliable

units. However, the utilization of these techniques for the purposes of evaluating and predicting the reliability of IC's is considered to be less promising.

Because of their merit, nondestructive methods are becoming increasingly popular and displacing traditional quality control methods from the production cycle, where these traditional methods have come to be of poor efficiency under modern production conditions [125, 126].

It is absolutely no accident that nondestructive testing tools have gained first place among the testing and quality control equipment planned for future years. In the semiconductor industry and in microelectronics, the demand for the development of new nondestructive quality control and physical and technical analysis tools as well as facilities for climatic and mechanical tests is characterized by a ratio of approximately 1:0.5:0.3.

Setting standards for the operational quality properties in standard setting engineering documentation for integrated circuits, which has been implemented in recent years and has become increasingly stringent since that time, as well as the relatively high production cost of these products and along with this, the undisputed advantages of nondestructive testing facilities - all of this is responsible for the constant work on improving them. Because of the improvement in the sensitivity and resolving power of these tools and the continuing improvement in the other metrological characteristics of devices of this class, they increasingly approach the level meeting the requirements placed on the standardized metrological characteristics from one variant to the next. The latter circumstance offers the real promise of making a transition in the near future to completely nondestructive testing in the category of quality control facilities, and to display equipment in the category of measurement facilities.

The Use of Test Structures. The quality control methods treated here do not provide for a complete estimate of the quality of large scale integrated circuits. It is practically impossible to check the elements of large scale integrated circuits in the majority of cases. One of the methods of testing such IC's is the testing of test structures, which contain individual structural components and make it possible to identify failures of the major components of an IC when the load is applied.

The design of test structures and the methodology of their application for purposes of quality evaluation and predicting the reliability of integrated circuits in the quality and reliability assurance of integrated circuits during the stages of design and fabrication will be described in more detail in Chapter V.

7. Acceptance Regulations for Series Produced Products

The acceptance regulations for series produced IC's provide for the performance of acceptance and quality control tests: acceptance and delivery, periodic, standard, qualification, selective quality control as well as durability and shelf life tests. The first group of tests include acceptance and delivery testing. Periodic, standard, qualification and selective quality control tests, along with durability and shelf life tests belong in the group of quality control tests.

Acceptance and delivery tests are performed for the purpose of checking the quality of the output product. For this reason, each batch of products from a production run are subjected to these tests.

The purpose of periodic tests is to check the constancy of the production process over a definite time segment. Integrated circuits are subjected to these tests which are fabricated during a reporting month, quarter, half-year, etc. The periodicity of the tests is established by the standard setting engineering documentation.

Periodic tests are also performed in the case of the renewal of the production of products following an interruption, the duration of which exceeds that permitted by the standard setting engineering documentation.

Standards tests are performed after introducing such changes into the production process for integrated circuits or into their design that they can influence the quality of the finished product. The task of these tests is to establish the conformity of the IC's to the requirements of the standard setting documentation after these innovations have been introduced.

Selective quality control tests belong to the category of quality control tests, by means of which the consumer of a product can check the work quality of the manufacturer practically within an unlimited range.

The goal of the tests for shelf life and durability, as follows from the names themselves, is to check the conformity of the IC's to the requirements of the technical specifications with respect to these indicators.

Qualification tests are performed when it is necessary to evaluate production readiness to produce integrated circuits of a certain series. Based on their results, the quality of the IC's of a setting batch is estimated and their acceptance is effected.

We shall treat the procedure and organization for the performance of the tests enumerated above in more detail as well as the rules for integrated circuit acceptance.

Qualification tests are performed on set-up batches of IC's. The program of qualification tests includes: checking the external appearance and quality of the marking of the IC's, monitoring the overall and connection dimensions, checking the static parameters (direct current parameters) of the products established by the technical specifications for the various test categories at the minimum, normal and maximum permissible temperature, as well as checking the dynamic parameters (alternating current parameters) at the normal temperature; testing the IC's for immunity to a cyclical temperature change, testing for strength when exposed to individual shocks and a centrifugal load; checking the hermetic seal; MTBF testing; testing the strength of the external leads; checking the suitability for soldering; checking moisture resistance; testing for vibrational strength and operational stability when exposed to vibrations; testing for impact strength when exposed to repeated shocks; checking the shelf life of the IC's at an ele-

vated temperature; durability testing; fungal immunity tests; testing for frost resistance; testing for immunity to a sea fog; testing for immunity to elevated pressure; testing for immunity to reduced atmospheric pressure; and testing for ability to withstand sound pressure (acoustic noise).

The program of qualification testing is not exhausted with this extensive list. It also includes limit tests, which provide for checking the margins of strength, resistance and immunity of the integrated circuits to mechanical, climatic, electrical and other loads. The strength of the packaging is also tested in the process of qualification testing.

Thus, in checking integrated circuit quality, a thoroughgoing check is made of production readiness to produce a product conforming to the requirements of the standard setting documentation which is in force. Based on the results of these tests, a decision is made concerning the start of series production of the particular type of product.

The test batch of integrated circuits intended for qualification tests is divided into groups, each of which is subjected to certain kinds of checks and tests. Its own acceptance number is established for each group in the technical specifications.

Upon the completion of all tests, a commission analyzes the results obtained. The reasons for failure are studied in the integrated circuits which failed. When a negative result is obtained (poor IC quality in the test batch), the IC manufacturer develops and implements measures to improve their quality. Samples with defects in the external appearance and marking are not taken into account. Integrated circuits fabricated after the implementation of these measures are again subjected to qualification tests. At the discretion of the commission performing the tests, this time the IC's can be checked only for those effects preceding the tests for which a negative result was obtained. It must be noted that exceeding the acceptance number in one of the groups is not a reason to terminate the tests. The tests are run through to the conclusion so as to obtain an overall evaluation of the batch being studied.

Limit tests of the IC's are usually performed simultaneously with the qualification tests for this same purpose. In this case, the margins of product stability with various kinds of loads, the margins of strength of the structural components are also ascertained, and the distribution of IC failures are established, if this is possible, with respect to the kind and degree of severity of the acting factors.

The tests are performed using the same methods and on the same equipment used in testing the strength and immunity of integrated circuits with individual types of loads. The difference consists in the test modes, the criteria for evaluating the results and the conditions for terminating the testing.

The use of thermal shock and thermal cycling, individual impacts of great force and centrifugal acceleration, high temperature storage as well as alternating and

constant electrical loading with the simultaneous exposure to the ultimate positive temperature is widely practiced as the loading during limit testing.

Considering the destructive nature of these tests, they are usually performed on a limited number of products (up to 10 units).

The test conditions are chosen by working from the posed problem as well as the design and production process features of the IC's being studied. It is recommended in this case that the following main rules be observed. The load steps are chosen taking into account the program and results of preceding tests of integrated circuits similar to those being studied in terms of the design and production process attributes (design and production process analogs). It is recommended that the initial step be chosen two steps lower than the one at which failures were obtained in the preceding tests. The duration of the exposure of the IC's to each tests mode is figured in hours.

The thermal parameters are determined at the maximum electrical power dissipated by the device. The ultimate values of the measurement temperature are specified in the technical specifications for the product or in the testing program.

Measurements of parameters being checked during the testing process are made at intervals of a definite number of cycles, specified in the technical specifications or in the testing program.

As a rule, the margins of IC ability to stand up to electrical loads are evaluated at the maximum ambient working temperature. The voltage, current or power is gradually increased in steps, starting at the nominal value. The value of the working temperature, the value of the load for each step and the duration of the exposure in each step are specified by the technical specifications or the testing program.

The safety margins in the ability of IC's to stand up to a constant electrical load are determined at a load level close to the ultimate value, established by the method indicated above. It is usually chosen 20% lower than the ultimate value. The ambient temperature in this case is chosen equal to the maximum working temperature specified by the standard setting documentation. It is recommended that the parameters be measured at time intervals of approximately four days.

Three single shocks are employed at each load step. The size of the load (the maximum acceleration and pulse width) are indicated in the technical documentation. The shocks are applied in a plane which represents the most dangerous direction for the IC's of the type being studied. A similar approach to the testing procedure is also realized with other kinds of mechanical tests.

The integrated circuits of each group are subjected to only one kind of test. The products which have failed are removed and analyzed for the purpose of establishing the cause of their failure.

The testing is terminated when the test program is exhausted, and the number of failed IC's does not exceed the permissible level, in other words, when confirma-

tion is obtained that the IC's are capable of standing up to the applied ultimate load. Another criterion for the termination of testing is the case of failure of half of the products being tested.

The rules for the performance of the tests authorize the termination of individual tests when a limit is reached at which half of the tested batch failed in the previous case.

Acceptance and delivery tests are performed as part of the quality control for each production batch of products. Selective single step quality control is employed as a rule. However, continuous monitoring is also used. This is usually practiced at the start of production of a certain series of IC's or when the previously registered level of quality of the output product has fallen off. A criterion for the assessment of the latter is an increase in the number of complaints.

Products received by the quality control section are turned over for testing. The accompanying documentation for a batch of IC's which have arrived for acceptance and delivery tests should contain information on the type and number of products in the batch, the date of batch manufacture and the date of presentation for acceptance testing, as well as the results of the tests performed by the quality control section. The integrated circuits are kept for a certain length of time under warehouse conditions between the acceptance by the quality control section and the acceptance and delivery tests.

In the case of selective quality control, the batches being tested are put together from different batches of IC's which are presented for acceptance testing. The number of products in a test batch should be sufficient to carry out testing with respect to all groups.

As a rule, the standard setting engineering documentation provides for no less than five test groups. One group provides for checking the external appearance and marking of the integrated circuits. Another provides for checking the overall and connection dimensions. The third provides for checking the static IC parameters in the case of the normal and ultimately permissible ambient temperatures in accordance with the technical specifications and dynamic parameters of IC's under normal ambient conditions. The fourth provides for a set of tests, which consist of checking the ability of the IC's to stand up to a cyclical variation in the ambient temperature, to linear loads as well as a check of the hermetic seal of the IC package. The fifth provides for testing the IC's under electrical load at the ultimate ambient temperature.

Each group provides for testing approximately the same number of IC's and an equal number of permissible failures. An exception is the fourth group, the tests of which are of a destructive nature, while the IC's subjected to these tests are excluded from the number delivered to the consumer. For these reasons, the number of IC's set aside for these tests is the minimum permissible.

The loads to which IC's are subjected during the testing process are specified by the technical specifications.

The breakdown into the first and second groups is more symbolic than of any substantial practical significance. Integrated circuits from one sample are usually subjected to these tests.

It is permissible to subject integrated circuits to testing in accordance with groups I, II, IV, V, which have passed the group III tests in the case of selective quality control.

Continuous monitoring of IC quality is accomplished in accordance with the group III program. The number of tested products in this case is figured in hundreds, among which, it is permissible to have individual samples which do not meet the requirements of the technical specifications. However, failures because of an open or short circuit in the electrical circuitry of the IC are not permitted at all. Checking of the external appearance and labeling is also included in the listing of the checks.

The acceptance rules provide for returning a batch of IC's to the manufacturer, if a negative result is obtained in the tests, even if only for one of the groups. It stands to reason that the issue involved here is more substantial defects than defects in the external appearance and labeling. Such IC's are simply rejected.

Various systems of applying sanctions to a manufacturer of a substandard product exist. One of the systems, for example, provides for terminating the acceptance of products, if of 10 production batches of IC's presented for acceptance have 3 batches in a row which were rejected in the process of the acceptance and delivery tests. In this case, acceptance is renewed only after receiving positive results for 3 batches in a row, the testing of which was preceded by a careful analysis of the reasons and sources for the rejection and failures, as well as the implementation of measures in production to prevent them.

The listing of the parameters to be monitored is established by the technical specifications.

Periodic tests are performed within timeframes established by the manufacturer in conjunction with the customer. This is usually once quarterly.

A test batch of integrated circuits for these tests is put together during a period of time between the previous and next checks. Included in the complement of a batch are only those products which have passed the acceptance and delivery tests.

Just as in the case of the acceptance and delivery tests considered above, a periodic testing program provides for several test groups. The test program for IC's in the first test group provides for repeating the tests covered by the first three acceptance and delivery groups. The difference consists only in the fact that these tests are completed with the check of the electrical parameters under dynamic conditions at the ultimate positive and negative temperatures. The second group of IC's is tested for immunity to exposure to individual impacts with an acceleration exceeding 100 g, as well as for moisture immunity. The third group of IC's are tested for MTBF for 500 hours at the ultimate positive

temperature. The fourth group of products undergo testing for the hermetic seal of the package, suitability for soldering, as well as the quality and strength of the external leads. A separate fifth group of IC's is singled out for testing of the moisture immunity during a longterm exposure.

The test sample for MTBF is made up of any one type from each group of the types of IC series being tested. Batches of IC's which represent any one type of products from one series are turned over for the remaining tests.

A positive outcome of periodic testing is considered to be the case where the tests of all groups of IC's were accompanied by a number of failures not exceeding that permitted by the technical specifications. Otherwise, the acceptance and delivery of the product is stopped. Work is done to ascertain the reasons for the excess number of failures. New technological approaches are worked out and introduced into production, changes are made in the IC design, new standards are set, etc. In a word, a set of measures is implemented which are called upon to prevent the appearance of an impermissibly large number of failures as compared to the value established by the standard setting engineering documentation.

An important place is set aside for limit tests among the methods of analyzing the reasons for an increased number of failures.

The rules for invoking sanctions provide for returning to the manufacturer all of the previously received batches of IC's which have not been unloaded, without the right of repeated presentation, if in the process of analyzing the samples which failed during the periodic tests it is determined that an elevated percentage of failures was due to a degradation of the fabrication quality or the use of materials, component products and semi-finished products which do not conform to the requirements of the standard setting documentation.

This rule does not apply if it is determined that the reason for an unsatisfactory evaluation of the test results is a defect in the equipment or an error by personnel.

The acceptance and shipping of products is renewed after the newly fabricated IC's successfully pass the tests. In this case, the tests are usually repeated only for that group for which a negative result was obtained.

Standard type tests are performed in accordance with a program which reflects innovations made in the production and design of the IC's. The composition of the quality control checks incorporated in a program of type standard tests depends on the nature of the changes which have been made, the degree of their possible impact on IC quality and the possibility of ascertaining this influence by means of the proposed methods. The program includes tests from among those figuring in the technical specifications for the product. However, this does not preclude using other kinds of tests also which can provide insufficient information, including comparative tests of different products.

An evaluation of the acceptability of the changes being introduced is made on the basis of the results of the type standard tests, taking into account the results of all the other tests.

Selective quality control testing is usually performed by the major customer for the products. The scientific research facilities of the customer are, as a rule, used in this case as the testing base. However, if mutually agreed on the tests can be performed at the manufacturer's also.

The volume of the tests is set in accordance with the desire of the customer and governed by the testing program. Samples for these tests are selected in accordance with the testing program from among those which have already been received by the quality control section. The testing timeframes and the procedure for their performance are established by the scheduling charts.

Tests for durability are usually performed as part of the qualification tests. It is considered sufficient to perform a durability check on any one type of IC from each group of types from a series. The selection of the type of products for the tests is the prerogative of the commission which receives the setting batch.

The commission usually performs these tests only for the first thousand hours. Then the tests are monitored by the quality control section.

It must be said that the practice of performing these kinds of tests which has come into being, which is supported by the standard setting engineering documentation, provides for combining the durability tests with the MTBF check of the integrated circuits. Having started the MTBF testing of the devices, the testing is finished with a check of the durability indicators. This is correct in all regards, and primarily in economic terms.

The duration of the durability testing stage is determined by the minimal mean time before failure of the IC's established by the technical specifications.

In the case where these tests are not a continuation of the MTBF tests and are performed independently, then the IC's selected for the indicated tests are preliminarily checked in accordance with the acceptance and delivery testing program. In this case, not all of the IC quality properties are checked, but only the absence of external defects, as well as the static and dynamic parameters. The static parameters, as is provided by the technical documentation, are measured at the normal, minimum and maximum temperatures. The alternating current parameters are tested under normal conditions.

Substandard integrated circuits, which are detected during the check process, are replaced with good ones. The rejected ones are forwarded to the failure analysis subdivision to determine the reasons for the rejection or the failure.

A result is considered to be a positive outcome of the durability tests when over the course of the minimum MTBF, the number of failed IC's does not exceed that permitted by the standard setting engineering documentation. A negative result of these tests entails an analysis of the causes of the failures as well as limit tests.

Shelf Life Tests. The following main goals are pursued in performing shelf life tests: the checking of the conformity of the IC's to the requirements of the standard setting documentation, the gathering of data on the technical shelf life, the more precise setting of standards for shelf life indicators and working out recommendations to improve storability.

Various testing techniques are employed to check the shelf life. The choice of the method is governed by the requirements placed on the operational characteristics of the IC's. Depending on the requirements, conditions are artificially created or selected, under which the IC's being studied are stored for a specified period of time.

The IC's are stored in heated or unheated repositories, under shelter or at an open air site. They are stored in standard packaging, or as components in equipment or sets of spare parts and accessories.

Integrated circuits are not tested in open air sites in the factory packing, since they are not adapted for this.

The heated room or storehouse with air conditioning should have a temperature set in a range of from +5 to +40° C and a relative humidity of up to 80% at a temperature of 25° C. The conditions of an unheated room are characterized by a temperature which varies in a range of from -55° C up to +40° C, and a relative humidity at standard temperature which does not exceed 98%. On open sites and under shelters, the permissible variation in the temperature fluctuates from -60° C to +50° C with a relative humidity of the environment under normal conditions of up to 100%.

The duration of the testing is specified in the standard setting engineering documentation. During this time, the electrical parameters of the IC's and their external appearance should remain within the range of the established norms. The norms are specified in the documentation for the starting point in time and the end of the tests.

The following rules are observed when choosing the IC type. Integrated circuits of any type are turned over for testing, which represent a group of series types. In the interests of attaining the maximum testing economy, it is permissible to group IC's of different types together. In this case, products are chosen which are representatives of the basic design, the standard fabrication technology or some other functional attribute. The results of the tests are extended to the entire class or group of products.

Here, just as in other cases, the samples for the testing are selected from a received batch by means of random sampling. Products having minor defects which exert no influence either on the electrical parameters nor on the evaluation of the external state of the IC are permitted to be subjected to this testing. Integrated circuits which do not conform to the requirements of the standard setting documentation are replaced.

The same parameters are checked during the testing process as during acceptance and delivery tests. It is recommended that the measurements be performed with

the same facilities during all tests. The probability of failure free storage or the percentage of good IC's following storage under specified conditions in an established time interval or within a definite storage time are taken as the criterion in evaluating whether the IC's are good.

Tests are also performed on IC's under natural conditions, storing them in different climatic zones and regions.

Shelf life tests at elevated and reduced temperatures are performed in heat and cold chambers. The IC's are de-energized when stored in them. The duration of the storage is figured in tens and hundreds (up to a thousand) hours. Integrated circuits for which the external appearance and electrical parameters following the testing conform to the requirements of the standard setting documentation are considered to have passed the test.

Failed IC's continue to be tested for a period of time necessary to determine the amount of the deviation of the parameters during the storage time. Upon the completion of the testing, the failed circuits are forwarded for analysis.

Chapter V. Ways of Assuring the Reliability of Semiconductor Integrated Circuits

Integrated circuit reliability is a comprehensive characteristic which is governed by an aggregate of many mutually related factors. The specified reliability level of integrated circuits is set during their design stage, and is assured during IC fabrication and maintained during their applications [27, 32].

The ultimately attainable level of reliability of integrated circuits depends on the selected design. It is specifically the design and production process variant of an IC which governs the strength safety margins of its components, the levels of the ultimately permissible loads (electrical, mechanical, climatic, etc.), and in the final analysis, IC reliability under its normal operating conditions.

The second major factor which determines the reliability level of an IC is the quality of the execution of the production process for its manufacture, selected for the realization of the design and production process solution established in the planning stage. In this case, reliability is assured by an entire set of measures, which includes primarily the following:

--A high degree of mechanization and automation of the production processes and quality control operations;

--Effective input quality control of the raw materials, semi-finished products and energy vehicles;

--High quality and efficiency in monitoring the observance of the technology and the maintenance of technological discipline at the requisite level;

--The presence of an effective automated control system for the technological production process based on statistical quality control of the production process using test structures;

--An effective production process testing system for the purpose of rejecting potentially unreliable products;

--Reliable monitoring of the level of quality and reliability of the finished IC's;

--Thorough analysis of the reasons for IC rejection and failure;

--Systematic development and implementation of measures to eliminate the ascertained reasons for failures during IC testing and operation, etc.

Finally, an exceptionally important factor which governs IC reliability during operation is the strict observance of all of the requirements of the standard setting engineering documentation for an integrated circuit in all stages of its application:

--During the design of the radioelectronic equipment (REA) using the IC's;

--During the input quality control of the IC's;

--In the stage of installing and debugging the modules and systems of the radioelectronic equipment;

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
WELDED CONTACT CONNECTION	Contact break in the region of a weld	Poor mechanical strength of the weld joint: poor weld strength ("sunk weld", unsatisfactory cleaning of the contact area (KP) [bonding pad - BP], small welding region area)	The use of "ball" thermal compression	Optimization of welding conditions. Improving the quality of opening windows in the oxide (glass) to the BP, intended for the welded contacts. Improving the quality of cleaning the chip surface prior to lead layout	Monitoring welding process parameters (temperature, specific pressure in the weld region, welding time). Monitoring the geometry of the working tip of the tool used for the welding (needle, capillary, etc.). Checking the completeness of oxide (glass) removal from a BP. 100% visual inspection under a microscope (magnification about 100x) of the chip for the absence of cracks, undercut etchings, mechanical damage to the BP. 100% visual microscopic monitoring of assemblies for the absence of mechanical damage to BP's,	Eliminating mechanical loads on the IC which are not permitted by the technical specifications, in all stages of IC application (input quality control, module assembly, equipment operation)	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
WELDED CONTACT CONNECTION					for the degree of deformation of wires and for the positioning of a welded contact on the BP (the "effective" weld area). Selective monitoring for mechanical strength of welded contacts (breaking force, displacement force, etc.). 100% production process testing of the finished IC's (centrifuging)		Effective only for IC's with gold wire leads
		Poor adhesion of the material of the bonding pad (BP) to the substrate	The use of sublayers of a metal which increase the adhesion of BP's to the substrate	Improving the quality of the preliminary cleaning of the plates prior to the application of metal film. Optimizing conditions for thin metal film	Quality control of the cleaning of the plates prior to metal application. Monitoring the application process (purity of the atmosphere, temperature of the substrate and rate of metal application). Checking the conditions for melting the metal during the stage of producing the ohmic contacts. Testing the adhesion of the metal film to the substrate.		

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
				application to a plate and the melting-in of the metal.			
WELDED CONTACT CONNECTION		The Kirdendall effect and the formation of transition metal compounds, Au_xAl_y, in the region of the weld	The substitution of single metal systems for the Au-Al bimetallic systems: a structure with "petal-shaped" leads (Al-Al system); a structure with "tab" leads (Au-Au system); the use of aluminum wire instead of gold; local gold plating of aluminum bonding pads	Reducing the temperature during thermal compression welding of gold wire leads to the aluminum BP's	Accelerated tests of test structures with Au-Al contact connections at elevated temperature or heat and electrical loads	Avoid long term operation or storage of the IC's at the maximum permissible temperatures of the technical specifications (T ≈ 125° C). The use of a heat sink to reduce the amount of chip overheating (especially for high power linear IC's and LSI circuits)	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
WELDED CONTACT CONNECTION	Wire lead break	Reduction of the wire cross-section close to the weld zone (the "heel").	The use of "ball" thermal compression. Use of structures with "petal-shaped" or "tab" leads	Working out conditions for the purpose of choosing the optimal degree of wire deformation	100% production process testing of the finished IC's (centrifuging)	Eliminating mechanical loads on the IC which are not permitted by the technical specifications in all stages of IC application.	
		Mechanical damage to wire leads			Output quality control of the wire intended for producing the weld connections to determine the absence of mechanical damage.		
		Great tension on a wire lead		The use of installations which guarantee the maintenance of the sag and preclude excessive tensioning of a wire lead when assembling the IC	Visual checking of the IC under a microscope. 100% production process testing (centrifuging)		The loads during the tests are applied in a direction which promotes the wire's tearing away from the chip

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
WELDED CONTACT CONNECTION	Intermittent break in a wire lead (in a plastic package)	Movement of the wire lead relative to the chip because of thermal expansion of the plastic			Input quality control of the wire. Visual checking of the IC wiring under a microscope. Checking the electrical parameters of the IC with a slow change in the ambient temperature		
	Short circuit (including an intermittent one) in the wire lead at the edge (corner rib) of a chip	Considerable tension on the wire lead	The use of a structural design (package) with a low position-ing of the chip relative to the contact pads of the feed-throughs. The use of dielectric (for example, polyamide) films which protect the surface of "petal-shaped" leads, turned towards the chip	The use of equipment which guarantees the maintenance of the required site sag of a wire lead during IC assembly	Visual checking under a microscope of the assembling of the IC's. 100% production process testing (centrifuging)		The loads during the tests are applied in a direction which promotes the pressing of the wire against the chip

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
WELDED CONTACT CONNECTION		Mechanical damage to a chip		Improving the quality of scribing and breaking the plates into chips	100% visual checking of the chips under a microscope for the absence of mechanical damage (sheared places, cracks)		
THIN FILM CONDUCTOR	Break of a thin film conductor	Local reduction in the cross-section area (mechanical damage to the film, unsatisfactory deposition of the metal on relief steps, the appearance of microcracks when melting the metal in to provide ohmic contacts, undercut etching of the metal,etc.).	Choice of the optimum ratio of the thickness of the metal films and the protective oxide. Elimination of the possibility of coincidence of the edges of the thin film conductors of the first and second levels (in order to structures with the oxide	The application of the metal using equipment with rotating substrates for more effective deposition of Working out photolithography conditions which provide for an acceptable slope to	Quality control of the metal film application (thickness, level of deposition of relief steps, etc.) with a scanning electron microscope (SEM)*. Quality control of the metal film at the boundaries of the contact windows (after melting-in the metal) with a SEM*. Monitoring the relief (the form of the steps) of the oxide with a SEM*. 100% visual inspection of the plates and chips with an	*SEM magnification: 10,000x to 30,000x. Selective quality control **The material and manner of dielectric film application are chosen from these

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			During IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	
THIN FILM CONDUCTOR			multilevel metallization). The introduction of a supplemental coating for the chips using dielectric films (to reduce the probability of mechanical damage to the metal film)**. The elimination of "bypasses" of the contact pads by thin film conductors (to reduce the probability of mechanical damage to them when checking the functioning in the plate and when assembling the IC).	steps when etching it. The introduction of a "smoothing" operation for the edges of the first level conductors in structures with multilevel metallization. Optimization of the conditions for melting the metal film.	optical microscope (magnification about 100x) for the absence of mechanical damage and undercut etchings of thin film conductors. Accelerated tests of test structures with thin film conductors, intersecting the maximum permissible relief steps, for exposure to direct (pulsed) currents at an elevated ambient temperature.		considerations: satisfactory mechanical strength; good surface protection of the chip against moisture and contaminants; the absence of a negative influence of the electrical parameters of the IC's.

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Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR		High level of current through a thin film conductor: complete burn-through of a conductor (when $J > J_{crit}$); electromigration of the thin film conductor material (at $2 \cdot 10^5$ amp/cm^2 $< J < J_{crit}$).	Optimal selection of materials used for thin film conductors: doping aluminum with silicon, magnesium and similar impurities; multilayer films (with sublayers of difficultly fusible metals) based on metals with a higher activation energy than	Application of the metal films using equipment with rotating substrates (to assure minimum gradients of the conductors at the relief steps). Optimization of the conditions for	Monitoring the conditions for the application and melting of the metal film to assure a large grained uniform thin film with good coverage of the relief steps. Quality control of the application and melting of the metal film using a SEM (film thickness degree of relief step coverage, the lack of	The exclusion of excessive electrical current spikes in the measurement and test equipment and accessories.	The exclusion of excessive electrical operating conditions (voltages, currents) in all stages of IC application: during input IC quality control, assembly of modules and electronic equipment operation. Reduction of the maximum temperature on the chip by means of incorporating a heat sink and reducing the ambient temperature in the electronic equipment units.

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	
THIN FILM CONDUCTOR			aluminum for the diffusion processes (Au, Mo, etc.). The introduction of additional passivating coatings for the metal film surface using dielectric films (SiO_2, Al_2O_3, etc.)**. Optimal selection of the geometric dimensions of the conductors when setting the design standards: increasing conductor width for the purpose of minimizing current density through the most "loaded" conductor (in the worst case) at a value	thin metal film application to assure the maximum possible grain size and homogeneity of grain structure. Optimization of the conditions for melting the metal film (in the stage of producing the ohmic contacts to the silicon). Working out the process steps). Accelerated tests of test structures with thin film conductors (single faces which does not degrade the structure of the metal film.	microcracks in a film at the boundaries of contact windows to the silicon, etc.)*. Checking the grain size of the thin film conductors. 100% visual inspection of plates and chips under an optical microscope for the absence of mechanical damage and undercut etchings of the thin film conductors (especially at relief steps).		*See the note on page 128 **See the note on page 128

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR			of $2 \cdot 10^5$ amp/cm^2; limiting the maximum permissible conductor length. Optimizing the configuration of thin film conductors (eliminating width gradients). Precluding the possibility of the matching of the edges of thin film conductors of the first and second levels (in structures with multilevel metallization). Reducing the temperature gradients at the chip surface and selecting IC designs which provide for the least heating of the chip relative to the environment during IC operation.		purpose of estimating the level of reliability (durability) of IC conductors and estimating the efficiency of the dielectric coating of conductors.		

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Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages			IC Application	Remarks
			IC Design	During IC Fabrication			
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR		Corrosion of the material of the thin film conductor with the action of contaminants and moisture: chemical corrosion of aluminum; electrochemical corrosion of materials in the region of a metal to deposited resistor contact.	Replacement of aluminum thin films with multilayer thin metal films based on gold. The choice of a single metal system for welded contacts to preclude their galvanic corrosion. The introduction of additional passivating coatings for the surface of the metal film using dielectric films (SiO_2, Al_2O_3, etc.)**.	Increasing the quality of cleaning the chips, the assembly and component packages prior to sealing the IC's. Eliminating the possibility of moisture and contaminants into the package. Providing sufficient oxide coverage of the edges of the contact pads under the welded contacts.	Quality control of the cleaning of the interior surface of an IC and the package components. 100% visual inspection of the dielectric film under a microscope for the absence of mechanical damage (during the photolithography of the windows on the contact pads). Testing the hermetic seal of IC's in all leakage rate ranges (slow, ing a high intermediate, degree of large leaks).	Assuring additional hermetic sealing of the units of electronic equipment to preclude the possibility of the intrusion of moisture to an IC surface. Eliminating mechanical and thermal stresses on IC's, which can cause a loss of package seal.	**See the note on page 128.

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Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			During IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR	Increased electrical resistance and breaking of the contacts between the conductors of different metallization levels.	Unsatisfactory quality of the interlevel contact: failure to open windows under contacts to the lower metallization level; partial undercut etching of the metal conductors of the lower metallization level; unsatisfactory coverage of the walls and "bottom" of the contact window.	The use of multilayer thin film metallic films (which assure more reliable contacts between the conductors of different levels and make it possible to choose more effective selective etchants for opening windows in the dielectric film).	Careful selection of the selective etchants and etching conditions in the window opening operation beneath interlevel contacts. Optimization of the conditions of assuring its uniformity in thickness. Application of the metal in equipment with rotating substrates.	Strict monitoring of the conditions for opening windows under contacts. Quality control of the window opening under contacts. Quality control of the application of the metal (film thickness and degree of coverage of the walls of the windows underneath contacts)*. Testing the electrical resistance of the contacts using test structures. Accelerated tests of test structures with contacts between different metallization levels for exposure to temperature and electrical loads.		*See the note on page 128.

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Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR		High current level through a contact.	Application of metallic films in equipment with rotating substrates (to assure minimal thickness gradients in the conductors at relief steps). Optimization of the conditions for applying the thin metal film to assure the maximum possible grain size and uniformity in its structure. Optimization of the conditions for melting in the metal film (in the stage of producing the ohmic contacts to the silicon).	Monitoring the conditions for the application and melting of the metallic film to assure a large grained uniform thin film with good coverage of relief steps. Quality control of the application and melting of the metal film using a SEM (film thickness, degree of coverage of relief microcracks in the film at the boundaries of contact windows to the silicon, visual inspection of the plates and chips under an optical microscope for the absence of mechanical damage and undercut etchings of the thin film conductors at		*See the note on page 128.

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	
					relief steps. Accelerated tests of test structures with multilevel metallization at elevated thermal and electrical loads to estimate the level of reliability (durability) of the IC conductors.		
THIN FILM CONDUCTOR	Shunting leaks and short circuiting of a thin film conductor to the substrate or another conductor.	"Smearing" of the thin film metal conductor (reducing the gap between the conductors of one metallization level).	The introduction of an additional coating of the chip using dielectric films**.	The introduction of vacuum tweezers for the purpose of preventing damage to the surface of the plates and chips by a sharp tool.	100% visual inspection of the chips and assemblies under a microscope for the absence of "smearing" of the metal conductors.		**See the note on page 128.
		Shorting the thin film conductor through microscopic holes or punched-through holes in a dielectric film: to the surface of the silicon substrate;	The introduction of an oxide surface (SiO_2) coating of a film of phospho-	Optimization of the conditions for producing the dielectric films on a surface:	Checking the level of the breakdown voltage of the dielectric film. Checking the density of microscopic holes in the dielectric film. Checking the quality of the		

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	
THIN FILM CONDUCTOR		rus-silicate glass (for the purpose of covering over defects, microcrystals, grain boundaries which extend out to the surface of the oxide).	using (where possible) low temperature film application, es for the interlevel insulation; using combined dielectric films (for example, RF sputtering with subsequent precipitation of SiO_2 from the gas phase).	application of the dielectric film of the interlevel insulation, especially at the edges of metal conductors (in structures with multilevel metallization) using a SEM*. The same, following the opening of windows under the interlevel contacts prior to deposition of the metal film of the next level*. Accelerated tests of test structures having multilevel metallization elements for exposure to thermal shocks and electrical loads to determine the dielectric strength and stability of the dielectric films.		*See note note on page 128.
			Smoothing the edges of the metal conductors to assure a low defect density in the protective film of the dielectric (interlevel insulation in structures with multilevel metallization). The				

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages			Remarks
			IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	
THIN FILM CONDUCTOR			choice of the optimum ratio of the thicknesses of the metal and dielectric films (interlevel insulation in structures with multilevel metallization). Reducing the thickness and width of the thin film conductors of the first interconnection level (with the condition that $J \leq 2 \cdot 10^5$ amp/cm^2) for the purpose of reducing the probability of cracking the protective dielectric film during thermal shocks.			

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THIN FILM CONDUCTOR		Electromigration of corrosion products on the surface of a chip.	The introduction of an additional passivating coating of the chip surface with a film of SiO_2 or glass (before or after the layout of the leads)**	Improving the quality of cleaning the chips, the assemblies and components of packages prior to hermetic sealing of the IC's. Precluding the possibility of the intrusion of moisture and contaminants inside the packages during the process of sealing during their hermetic sealing.	Quality control of the cleaning of the internal surface of an IC and the package components. 100% visual inspection of the dies to the electric film under a microscope for the absence of mechanical damage and undercutting etchings (during photolithography of the windows on the contact pads). Checking the hermetic seal of the IC through the entire range of leakage rates (small, intermediate and large leaks).	Providing additional hermetic sealing of radio equipment units to preclude the possibility of moisture getting to the IC surface.	Observed in the case where gold thin film conductors are used. **See the note on page 128.

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
THE METAL TO SEMI-CONDUCTOR OHMIC CONTACT	An increase in the electrical contact resistance and break of an ohmic contact.	High current level through the ohmic contact: local overheating of an ohmic contact; thermal diffusion of the silicon into the aluminum ("peeling" of the aluminum conductors). Unsatisfactory quality of the "opening" of the windows underneath ohmic contacts (incomplete removal of the oxide film).	Replacement of thin aluminum films with multilayer films having substrates. The difficultly fusible metals (Mo, Ti, $PtSi_2$), especially in IC's with small junctions. Taking into account the effect of displacement of the "current" in the ohmic contacts in the calculation of	Improving the quality of opening windows in the oxide under the ohmic contacts of the metal application and melting of the metal film to provide for good optimization of coverage of the conditions oxide steps with for melting in the metal. Doping the aluminum with silicon (prior to the deposition), especially in	Quality control of the opening of the windows in the oxide under ohmic contacts (visual, cathodic inspection, etc.). Checking the conditions for the application and IC's, assembly of the units and operation of the contact windows).	Precluding the exceeding of the electrical conditions (voltages, currents) in all stages of IC application: during input quality control of the IC's, assembly of the units and operation of the radio electronic equipment. Reduction of the maximum temperature at the chip by means of introducing a heat sink and decreasing the ambient temperature in the electronic equipment units.	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages: IC Design	During IC Fabrication: Improving the Production Process	During IC Fabrication: Improving QC and Rejection Methods	IC Application	Remarks
THE METAL TO SEMI-CONDUCTOR OHMIC CONTACT	Short circuiting of the p-n junction (melting through the silicon).	A high current level through the ohmic contact: electromigration of the silicon into the aluminum and the melting through of the diffusion region with a eutectic alloy, especially in structures with fine (1 μm) p-n junctions. The reduction of silicon dioxide to silicon (because of the reaction of Al with SiO_2).	the optimal contact area (increasing the width and increasing the length of the contact). The introduction of additional passivating coatings of the metal film surface with dielectric films (SiO_2, Al_2O_3, etc.)**.		Checking the quality of the application and melting of the metallic film by means of a SEM (degree of coverage of an oxide step and the lack of microscopic cracks in the film at the boundaries of the contact windows to the silicon; the lack of local silicon melt-throughs in the area of the ohmic contact; the lack of undesirable changes in the structure of the metal film, etc.)*. Checking the electrical resistance of the ohmic contacts using test structures. Accelerated tests of test structures with ohmic contacts to the silicon at elevated temperature loads to estimate the quality and stability of the ohmic contact properties.		*See the note on page 128. **See the note on page 129.

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
DIELECTRIC FILM	Increased leakage currents	Contaminated surface of the dielectric film ("ion" type leaks).		Careful cleaning of the chips, assemblies and package components of contaminants. Increasing the quality of the hermetic seal of the packages. The use of "clean rooms" (protective suits).	Checking the quality of the cleaning of the surface of chips, assemblies and internal surfaces of package components for the absence of "ionic" contaminants (chlorine, sodium, etc.). Checking the hermetic seal of the IC's throughout the entire range of leakage rates (small, intermediate and large leaks).	Additional hermetic sealing of electronic equipment units to preclude the possibility of moisture getting to the surface of the IC's. Eliminating mechanical and thermal stresses on IC's, which can cause a loss of packages.	
		Contaminants and defects of the dielectric film: inversion type leaks; instability of the properties of the $Si-SiO_2$	The introduction of stabilizing films (for example, phosphorus silicate glass - PSG), getting out the technology for the application of these films	Working out the purpose of assuring the specified properties of the PSG (P_2O_5 concentration, PSG thickness, etc.). Monitoring the mobile	Checking the conditions for emitter diffusion for the purpose of assuring the specified properties of the PSG (P_2O_5 concentration, PSG thickness, etc.). Monitoring the mobile		

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
DIELECTRIC FILM		separation boundary (the level of the threshold voltage for a MOS structure) due to migration of cations in the volume of the dielectric film.	ter cations of alkali metals (contamination). Accounting for the influence of the methods and conditions for the application of passivating films of interlevel insulation on the stability of the properties of the Si-SiO_2 separation boundary.	ing the optimal concentration of P_2O_5 and thickness of the PSG. Improving the quality of the cleaning of the plates prior to the application of the dielectric film. Working out the process of applying a dielectric film which assures its high quality (a small number of mobile charge, perfection of the dielectric structure, etc.). The use of "clean rooms" (protective suits) with improved parameters of the working atmosphere.	charge in the dielectric film (using test structures) which is due to contaminants and defects. Accelerated tests of test structures (with elements of MOS structures) for exposure to heat treatment in the presence of an electrical bias, to estimate the stability of the MOS structure and the "sensitivity" of the IC to the appearance inverse conductivity channels at the surface of the semiconductor chip.	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
	Short circuit (dielectric breakdown)	Low dielectric strength of the films.	The same methods as in the section "Thin Film Conductor" (see the entry "Shorting of the thin film conductor through microscopic holes and punch-through holes in the dielectric film").				
DIELECTRIC FILM		Exceeding the maximum permissible voltage level (intensity in the dielectric film): voltage spikes (during testing and operation); static electricity discharges.	The introduction of the possibility of additional voltages to the IC (especially LSI circuits and IC's using MOS structures), which protect them at the inputs, etc.).	Precluding of applying equipment and elements in the IC (protective diodes, limiting resistors implementation of technical specification section). The	Certification of measurement and test voltages for accessories for the absence of electrical voltage spikes. tests (including production process test-ing) which exceed those permitted by the manufacturer- technical specification for the IC's against static electricity discharges during their fabrication and testing: grounding equipment and accessories; introduction of measures to protect the IC's against static electricity discharges in all stages of IC applications.	Eliminating the possibility of applying voltages to the IC leads in all stages of application (input quality control, unit assembly, electronic equipment operation), which exceed the maximum permitted by the technical specification section for the IC. The implementation of measures to protect the IC's against static electricity discharges in all stages of IC applications.	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
DIELECTRIC FILM					ducing "grounded" bracelets for operators; transporting the cassettes with the IC's only where "shorting inserts" are present, which bridge all of the IC leads; maintaining the humidity in the production atmosphere at a level which prevents the accumulation of high static electricity potentials on equipment and personnel, etc.		
ACTIVE AND PASSIVE ELEMENTS OF A SEMICONDUCTOR CHIP	Short circuit of an element	Breakdown of a p-n junction because the permissible electrical load levels are exceeded.				The same methods as in the section "Thin film conductor" (see the entry "High current level through a thin film conductor - complete conductor burnup").	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
ACTIVE AND PASSIVE ELEMENTS OF A SEMI-CONDUCTOR CHIP		Junction defects: "false" ("parasitic") diffusion of a doping impurity (because of defects in the photolithography); reduction in the level of the breakdown voltage (because of a disruption of the diffusion profile); defects in the crystalline structure of the semiconductor material (the epitaxial layer), etc.	Taking the possible influence of structural defects into account as well as the extent of the plate structured doping on the characteristics of the diffusion regions and the stability of their properties when selecting the original material for the IC.	Improving photolithography quality for the purpose of preventing undercut etchings of the oxide and contamination of templates. Quality control of the photolithography. Monitoring the photolithography. Monitoring the parameters of diffusion ing out diffusion and oxidation conditions: strict conformity of the junctions. Quality control of the p-n fusion regions junctions: breakdown voltage level, form of the voltampere characteristics, level of leakage currents.	Monitoring the diffusion conditions (temperature, time, gas flow rate, etc.). Quality control of the photographic templates. Quality control of the regions (including the use of test structures and satellites): impurity concentration and distribution. doping depth of the p-n junctions. Quality of the p-n ampere characteristics, level of leakage currents. (with densities	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
				exceeding the permissible level).			
ACTIVE AND PASSIVE ELEMENTS OF A SEMICONDUCTOR CHIP	Instability of the electrical parameters of active elements	Change in the characteristics of the diffusion layers (especially in heavily doped "small" p-n junctions).	Taking into account the gradation of the properties of small junctions when determining the limits of the permissible scatter in the parameters of transistor structures.	Refining the diffusion production processes (including the production of small junctions) for the purpose of assuring high reproducibility of the electrophysical parameters of active elements of IC's.	Monitoring the density of dislocations in semiconductor materials. Checking the characteristics of active elements using test components.		
		Punch-through breakdown in transistor structures (because of defects in the photolithography and diffusion). Increased sensitivity of the	The choice of the optimal doping level for base regions of transistors.		Monitoring the electrophysical parameters of diffusion layers and transistor structures (the doping depth of p-n junctions, surface concentrations and distributions of doping impurities, the base width of a transistor, etc.). Accelerated		

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
		transistors to inversion of the conductivity (because of a low doping level of a p-type base).			tests of test structures with active elements for exposure to elevated thermal and electrical loads to check the stability of their electrophysical parameters.		
CHIP TO CHIP HOLDER CONTACT	Separation of the chip from the chip holder	Poor mechanical strength of the contact connection: small effective chip to chip holder contact area (because of a large number of cavities and holes in the eutectic or glued connection, skewing of the chip during seating, etc.). Mechanical overloads on the IC's when they are used.	Predominant utilization of eutectic alloys for seating instead of glued contact joints.	Refining the conditions for the chip to chip holder seating operation in the package for the purpose of assuring the maximum mechanical strength of the contact and minimal thermal resistance for the IC.	Monitoring the parameters of the production process of chip to chip holder seating. Checking the mechanical strength of the chip to chip holder contact joint using test samples (selective: for shear, etc.) as well as finished IC's (100% centrifuging). 100% visual inspection of the quality of the seating of the chip in the chip holder of the package.	Precluding the application of mechanical loads to the IC which are not permitted by the technical specifications in all stages of IC applications.	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
	High thermal resistance of the IC.	High thermal resistance of the chip to chip holder contact (small effective contact joint area, large thickness of the glue layer in the case of a glued joint, etc.).	The same methods as in the preceding section.				
CHIP TO CHIP HOLDER CONTACT							
IC PACKAGE	Poor hermetic seal of the IC package.	Unsatisfactory quality of the welded or sealed seam.	Predominant utilization of IC types which are hermetically sealed by welding.	Refining the conditions for sealing IC's to assure conformity to the technical specifications (with respect to the hermetic seal, external appearance of the IC's, etc.).	Input quality control of the packages for conformity to the requirements of the technical specifications (including the absence of places and other mechanical damage	Precluding mechanical and thermal loads on the IC which are not permitted by the technical specifications, in all stages of IC applications.	It is necessary to assure conformity of the technical specifications for packages to the requirements of the technical specifications for the IC's.

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				
			IC Design	During IC Fabrication		IC Application	Remarks
				Improving the Production Process	Improving QC and Rejection Methods		
IC PACKAGE	Cracks at the sites of glass insulators.		Optimizing the techniques and conditions for the application of supplemental protective dielectric films to provide maximum protection of the chip surface (assembly) of the IC against exposure to possible contaminants and moisture.	Checking the IC assemblies prior to hermetic sealing for the lack of foreign particles and damage to components. Checking the conditions for the sealing of the IC's. Checking the hermetic seal of the IC's throughout the entire range of leakage rates (small, intermediate, large leaks). Visual inspection of finished IC's (for the lack of mechanical damage, dirt and corrosion of package components, etc.).	to components; the thickness and quality of the metal coatings of components; the hermetic seal of the bases, etc.).	Careful washing of contaminants from the IC's during their installation in electronic equipment units. Additional hermetic sealing of electronic equipment units for the purpose of preventing the exposure of IC's to elevated ambient humidity. Storage of IC's in special kits in moisture-proof packing.	

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
IC PACKAGE	Corrosion of package components.	Unsatisfactory quality of the coatings of metal packages (gold, nickel, etc.): small coating thickness; the presence of pores, microcracks, incomplete coverage; mechanical damage to the coatings. Chips off of glass insulators, exposing portions of metal components of the package which are not coated.	Predominant use of ceramic packages with external leads made of corrosion resistant materials.				
	Leaks and corrosion of thin film conductors due to poor moisture immunity of an	Poor protection of the chip against the intrusion of moisture.	Choosing molded compositions with increased moisture immunity. The introduction of supplemental protection for the surface of a chip or assembly				

TABLE 20 The Major Kinds and Causes of Semiconductor Integrated Circuit Failures and Ways of Eliminating Them

Structural Component Responsible for IC Failure	Kind of IC Failure	Reason for IC Failure	Methods of Eliminating Ascertained Reasons for IC Failures in the Following Stages				Remarks
			IC Design	During IC Fabrication		IC Application	
				Improving the Production Process	Improving QC and Rejection Methods		
IC PACKAGE	IC in a plastic package.		using dielectric films (silicon dioxide, glass, etc.).				
	Short circuits or breaks.	Poor mechanical strength of the package structure. Damage to package components. Intrusion of foreign particles into the package.	Predominant utilization of DIP packages.				

--During the process of operating the radioelectronic equipment.

In a first approximation, the ways of eliminating the major sources of IC failure were mentioned in Chapter 3, which was devoted to a discussion of the kinds, causes and mechanisms of IC failures. We shall consider the factors which have an impact on IC reliability in more detail, as well as ways of boosting reliability in all stages of IC design and applications.

In Table 20, which is compiled based on the generalization of extensive statistical testing and operational data on IC's, the analysis of failed IC's and numerous research studies of the causes and mechanisms for their failures (see Section III), the major ways of improving the reliability of individual structural components are indicated which determine IC reliability as a whole during IC design, fabrication and application.

8. Integrated Circuit Reliability Assurance During Design

Assuring a definite reliability level during the design stage can be achieved only with the condition that such a production process is chosen that the major factors which have an impact on the reliability of integrated circuits of the particular class are thoroughly taken into account:

--The requirements placed on the electrical insulation of the individual circuit elements;

--Optimal methods of fabricating internal circuit contact connections and assuring their reliability;

--Production process scatter and instability in the parameters of the active and passive components of an IC;

--The production process suitability and maximum possible degree of automation of a given fabrication process, assuring the production of products of uniform quality, etc.

Besides the selection of the optimal technology, the choice of the optimum IC design is of extraordinary importance, where this selection is made taking into account the dominant kinds and mechanisms for failures characteristic of the given class of IC's. The following play a great role in this respect:

--The correct choice of the raw materials for the fabrication of the planar structure;

--The optimal selection of materials and methods of applying dielectric films for various purposes (passivating, electrical insulating, protective films, etc.) for the purpose of assuring reliable electrical insulation of the elements from each other, protecting the structural components against mechanical and chemical damage (corrosion) and stabilizing the chip surface;

--The use of special methods directed towards preventing the occurrence of surface inverse conductivity channels, and accounting for the possible instability of IC parameters due to phenomena at the surface of the chip and at the $Si-SiO_2$ separation boundary;

--The optimum selection of materials, designs and production processes for producing the contact connections - thin film conductors and resistors, ohmic

contacts to the silicon and welded contacts of flexible conductors to the chip and package feed-throughs; (it is necessary in this case to first of all use those metallurgical systems which make it possible to eliminate negative phenomena related to the possibility of the formation of undesirable transition metal compounds in regions of contacts between different kinds of materials ("gold--aluminum", "aluminum--chromium", etc.); secondly, use such metals or multilayer films for the formation of thin film conductors which allow for a substantial reduction in the probability of electromigration of the metal, as well as chemical and electrolytic corrosion of the materials);

--Optimization of the configuration and geometric dimensions of thin film conductors (the absence of sharp gradients over the width of the conductors; minimization of the current density by means of widening the conductors, especially in the most "loaded" sections; avoiding conductors with a length exceeding the "critical" value, eliminating "bypasses" of the contact pads by thin film conductors, etc.).

Moreover, it is essential to correctly choose the following:

--The spacing between individual elements and the distance from them to the edges of the chip;

--The manner of fastening ("seating") the chip to the chip holder of the package, which assures adequate mechanical strength, low thermal resistance of the contact and immunity to mechanical stresses during thermal cycling, which occur because of the differences in the temperature coefficients of the materials which are in contact;

--The structural design of the package, which assures a low thermal resistance for the IC, a good hermetic seal and structural strength, as well as high corrosion resistance, which guarantees IC reliability when operated under such environmental conditions as elevated humidity, a sea fog, etc.

During the design stage, it is also necessary to provide for a sufficient safety margin with respect to the IC parameters, which makes it possible to assure its reliability for a specified time given the condition of a certain instability in the values of the electrical parameters of individual components during IC operation in a permissible range of ambient temperatures. An important factor in assuring reliability during the design stage of an IC is the widescale utilization of basic technological processes to realize the selected IC design. This makes it possible to most fully utilize all of the advantages which are provided by comprehensive standardization and unification.

As an example which illustrates the complexity of the problems confronting the designer and developer of an IC, we shall cite the widely known problem of assuring the reliability of contact connections between the chip and the package feed-throughs [27, 44, 129-132]. The basic difficulty consists in having a comprehensive approach to the solution of the given problem. One of the cardinal methods of preventing the formation of undesirable transition metal Au_xAl_y compounds in the welded contacts of integrated circuits is the utilization of single metal systems to produce the contact connections in the IC's.

The use of a IC design with "tab" leads [28,130, 131] is promising in this regard. Chips with thin film multilayer conductors based on gold with sublayers of different metals (platinum, titanium, palladium), needed to assure reliable ohmic contacts to the silicon and high adhesion of the conductors to the substrate (Figure 30) are used in this IC structural design. So-called "beams" [tabs], electrolytically thickened extensions of thin film gold leads, extending out beyond the edge of the chip, are used to make the contact connections of the chips to the package conductors. The chips are mounted on the ceramic plates of the "working" surface downward, while the tab leads are connected to the gold thin film interconnections of the plate by means of thermal compression. A completely single metal, extremely reliable system of metallic contact connections is obtained as a result.

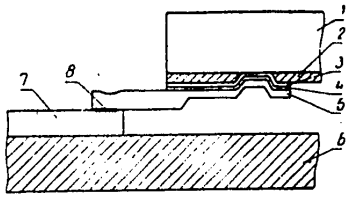

Figure 30. Schematic drawing of an integrated circuit with "beam" leads.

Key: 1. Chip; 2. Dielectric film; 3. Titanium; 4. Platinum; 5. Gold; 6. Plate; 7. Current conducting gold track; 8. Welded contact.

A second method of eliminating the possibility of the formation of Au_xAl_y transition metal compounds at the contact pads of a chip is dispensing with gold as a material for the wire leads in favor of aluminum. However, one must take into account in this case the fact that since it is necessary to create contacts not only to contact pads on a chip, but also to package feed-throughs in any integrated circuit, then just replacing the gold leads with aluminum ones will not alone completely solve the problem of eliminating transition metal compounds in integrated circuits sealed in packages with feed-throughs made of gold plated Fernico.

In this case, it is necessary to replace the material used for the package feed-through with a different one which does not yield transition metal compounds in contact with aluminum which have undesirable properties (brittleness, increased electrical resistance, etc.).

An IC structural design with petal shaped leads [132, 133] made of aluminum foil has been developed at the present time for this purpose.

The insulation of the petal shpaed leads on the chip side with an elastic polyimide [sic] film possessing good dielectric properties is used in this IC structural design for the final solution of the problem of preventing short circuits of the wire leads at the edge (corner) of the chip (region 5 in Figure 31). The use of a polyimide film makes it possible to simultaneously overcome difficulties related to the necessity of mounting the chips in a package with a low positioning of the feed-throughs (relative to the "working" surface of the chip) in a number of cases. By way of example, one can point to the structural design of

multiple chip VLSI circuits, in which the chips are mounted on a ceramic plate with thin film conductors applied to it as the interconnection wiring between the chips.

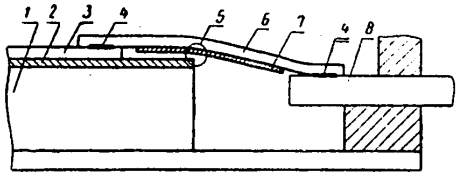

Figure 31. Schematic drawing of an integrated circuit with petal leads.

Key: 1. Chip; 2. Dielectric film; 3. Thin film aluminum conductor; 4. Welded contact; 5. Edge of the chip; 6. Aluminum petal shaped lead; 7. Polyamide film; 8. Package feed-through.

To simultaneously eliminate the corrosion of package components, it appears promising to use ceramic cup type DIP packages with corrosion resistant external leads (feed-throughs), made from an alloy which does not yield undesirable transition metal compounds with aluminum, which is used in the given structural design as the material for the flexible internal leads of the IC [137].

Another example of the broad possiblities open to an IC developer as regards the selection of ways of improving IC reliability can be the classical problem of aluminum metallization at relief steps with its tendency towards failures because of electromigration [27, 28, 139, 140].

To exclude this failure mechanism under actual conditions of long term operation of high power IC's with an elevated ambient temperature, the IC designer has an entire arsenal of techniques available to him (see Section III and Table 20):

--Improve the effectiveness of the coverage of steps by means of applying aluminum in equipment with rotating substrates or by deposition of aluminum on a stationary substrate from several sources;

--"Smoothing" the SiO_2 relief by means of etching it in a buffered etchant (which is not desirable of the sharp degredation of the electrical insulating properties of the oxide film) or by preliminary "smoothing" of the edges of the conductor of the lower layer of metallization (which leads to a substantial reduction in the cross-section of the thin film conductors of the lower level of metallization and should be compensated with a corresponding increase in their width);

--Quality control of the coverage of steps by means of studying each plate in a scanning electron microscope;

--The utilization of other quality control techniques for the coverage of steps with metal and the immunity of the thin film conductors to electromigration processes (for example, accelerated tests for the purpose of quality control of thin film conductors, which are performed on test structures: testing based on the current pulse level which leads to a conductor failure, or testing under forced thermal and electrical loads);

—Selecting an aluminum application technique which assures a large grained homogeneous structure for the metal film;

--The introduction of additional surface protection for the aluminum conductors with a thin film dielectric (SiO_2 or Al_2O_3), however, one must take into account the fact that to assure more effective protection (including anticorrosion) of the entire ship surface, it is preferable to apply an SiO_2 film, since, as a rule, an Al_2O_3 provides only for local protection of the aluminum; on the other hand, it must be kept in mind that MOS sturctures are more critical to the application of SiO_2, and protecting the aluminum with an Al_2O_3 film is more promising for them;

--Using aluminum doped with impurities which reduce the electromigration rate (silicon, magnesium, etc.);

--Dispensing with aluminum as a material for thin film conductors and replacing it with multilayer films based on gold, molybdenum and othermetals with a higher activation energy for the electromigration process.

Depending the specific requirements placed on IC reliability, the conditions for IC application (temperature at the chip, maximum current density in the worst case, etc.) and the limitations on integrated circuit cost as well as limitations imposed by other IC structure components or other failure mechanisms, the designer makes a compromise decision which though it does not reduce electromigration to zero, still substantially minimizes this undesirable process.

9. Assuring IC Reliability During Their Manufacturing Stage

We shall consider yet another factor which governs integrated circuit reliability: observing the technology layed down during their planning in the production stage. The main goal of production quality control is the assurance of a satisfactory and stable quality and reliability level for the IC's by means of a carefully thought out checking of the production process for their fabrication [27, 32, 113, 120].

Production quality control, as has already been noted, is accomplished through the comprehensive application of different techniques. The main ones of them are:

--Input quality control of the raw materials, semi-finished products and complete components;

--Quality control for conformity of the production process parameters to the requirements of the production process documentation (including the state of the working atmosphere, the conformity of the production process equipment, working tools and accessories);

--Intermediate quality control of batches of plates (using "working" plates, "satellites", test structures) between operations ("operation by operation");

--Production process tests and rejection;

--Systematic quality control of the finished product for conformity to the requirements of the standard setting documentation for the IC's.

We shall treat the indicated methods of IC reliability and quality assurance during the process of manufacturing them in more detail.

In summing the results of analyzing IC's which failed during various tests, a conclusion can be drawn that the major causes of typical failures are:

--Nonconformity of the quality of the raw materials, semi-finished products and complete components to the requirements of the designer and production process documentation for the IC's'

--Deviations from the technology, which occur during the process of fabricating the IC's because of operator errors, errors in the production process and monitoring and measuring equipment, poorly worked out individual operations in the production process cycle or insufficiently ineffective quality control and rejection of products with hidden defects [27, 32, 115, 138, 141].

Input quality control of the materials, semi-finished products and complete components used in IC manufacture makes an important contribution to reliability assurance of the IC's [27, 141]. During the input quality control step:

--Microcracks, crystallographic imperfections and other defects are found in the plates of the starting semiconductor material and are tested for the value and uniformity of their electrophysical parameters (thickness, specific resistance of the epitaxial film (based on the plate area), the distribution of impurities over the depth of the layer, etc.);

--Defective IC packages, having cracks and sheared-off placed in the glass insulators are detected and rejected in a timely manner as well as nonconformity of the thickness and quality of the metal coatings to the requirements of the engineering documentation, mechanical damage and contamination of package parts, etc.;

--Mechanical damage and other defects of the gold and aluminum wires used as the material for the flexible leads of the intracircuit wiring are ascertained;

--The conformity of the quality of the chemical materials (acids, bases, organic solvents, photoresists, etc.) as well as the energy vehicles used in IC production to the requirements of the engineering documentation is determined;

--Defective glass plates intended for thefabrication of photographic templates, which are an exceptionally important tool used in IC production are detected and rejected, etc.,

i.e., a complete check is made of the incoming materials, semi-finished products and complete components to assure that they are up to standard: that their parameters conform to all of the requirements of the standard setting engineering documentation.

Nonconformity of the quality of delivered packages and epitaxial layers [137] to the requirements of the technical documentation for the integrated circuits represents the greatest danger from the viewpoint of reliability. Thus, for example, numerous types of packages do not stand up to exposure to the production process conditions of assembly (such defects as unsatisfactory quality of the welded contacts to the feed-throughs, peeling away of the metal coatings of the leads, chips in the ceramic and glass insulators, etc. appear during the assembly process), and do not meet the requirements of the quality control section for the integrated circuits as regards moisture immunity, mechanical strength, shelf-life under field conditions at elevated temperatures or stability to exposure to other environmental factors.

In this regard, it is of exceptional importance to assure such a situation that the requirements of the standard setting engineering documentation for all materials, semi-finished products and complete components used in the production of IC's are no less stringent than the corresponding requirements of the standards setting engineering documentation for the IC's. This in turn requires coordinated actions by suppliers of the raw materials and complete component products for IC's as well as designers and manufacturers of integrated circuits.

Only in this way can a solid basis be created for the manufacture of a product of a specified level of quality which is uniform in terms of its properties and characteristics.

One of the effective ways of assuring the output of high quality integrated circuits is improving the level of production process quality control.

A significant number of IC failures is related to an unsatisfactory condition of a planar structure surface, defects in metallization and welded contact connections. The causes of such defects are most often damage to and contamination of the planar structure and structural components of an IC, which are caused by violations of production conditions:

--Violation of the requirements for vacuum hygiene at the work positions;

--Elevated humidity and dust contents of the working atmosphere;

--Insufficiently careful washing of the plate with the structures prior to the main operations of diffusion, oxidation and photolithography;

--Insufficient drying and cleaning of the vehicle gases, and the oxygen used in the diffusion and oxidation processes;

--Careless handling of plates and photographic templates during their transportation and work operations in IC fabrication;

--Insufficiently careful preliminary treatment of the vaporizers used for the vacuum application of thin film IC elements;

--Poor quality control and untimely replacement of photographic templates, tools and fittings, used during the assembly operation, etc.

All this leads to the fact that the grown oxide film can contain a significant number of defects (pinholes, microcracks, impurities and foreign particles, introduced into the oxide, etc.), which reduce its electrical strnegth or expose the silicon surface, something which leads to the occurrence of shunting leaks and short circuits of the thin film conductors of various levels to each other or to the surface of the silicon in the defective regions of the planar structure. Moreover, the presence of the indicated defects leads to the appearance of diffusion tubes and other defects, related to "parasitic" ("false") diffusion at points of local bear places on the surface of a semiconductor plate.

The contamination of the oxide surface or the presence of impurities and contaminants in the oxide film itself degrades its masking and passivating properties, unavoidably leads to the increase in leakage currents shunting the p-n junctions, promotes the formation of surface channels with inverse conductivity, and as a consequence, brings about gradual conditional and even complete failures of the integrated circuits during their testing and operation.

Another source of surface contamination is gas and moisture absorption by the planar structure surface, which leads to the apperance of charges in the near surface regions of the oxide film, which also serves as a cause of the subsequent occurrence of surface channels in the active elements of integrated circuits.

Increasing the quality of purification of the chemical reagents (acids, bases, organic solvents, etc.), the deionized water and vehicle gases, as well as the filtering of the photoresists used in the production of the integrated circuits, the use of special cabinets and "clean", which assure improved parameters of the working atmosphere and the basic operations of the technological process of fabricating the IC's (especially during photolithography and loading the plates into diffusion furnaces); strengthening the quality control of the parameters of the atmosphere in production rooms, the purity of plate surfaces and IC chips, etc. - all of this together makes it possible to substantially reduce the density of defects and charge level in an oxide, as well as the contamination of chip surfaces and package components and improve the quality and reliability of integrated circuits, especially very large scale integrated circuits.

Careless handling of plates and chips, the use of unprotected metal tweezers with sharpened working surfaces in production, rough setting of the probes when checking

the functioning during the stage of quality control rejection of structures on plates, which is accomplished using a microprobe manipulator also cause failures of IC's because of mechanical damage to thin film conductors and contact pads.

Inadequate checking of the geometry of the working areas of needles and other tools used to weld flexible leads to a chip and to feedthroughs of an IC lead to a violation of the welding conditions, since the specific pressure in the region of the weld contact in this case is practically uncontrolled. A result of this is either poor mechanical strength because of incomplete welding of the welded contacts, or overwelding and a small contact joint area. Both of these lead to breaks in the contact connections under certain conditions.

A cause of failures related to local overheating of chip components, separation of the chip from the base (the chip holder) of the package, and short circuits of the wire leads to each other can be the careless seating of the chip or incorrectly lining it up during mounting on the IC package base.

Since a significant percentage of the observed failures is related to operator errors and inadequately objective quality control during individual IC assembly and sealing operations, possibly more complete replacement of manual labor with mechanical operation and automation in the indicated production process operations are effective methods of reducing the failure rate and improving IC reliability.

An important means of boosting IC reliability is effective quality control of the products and major parameters of the production process between operations and establishing correlation functions between them based on the determination of the major criterion parameters for IC reliability.

The reliability criterion parameters include both the electrical parameters of the finished IC and the electrophysical characteristics of the individual components of its structure (including the planar structure chip).

A systematic comparison of the results of testing between operations with the mean statistical indicators of the process and the results of IC reliability tests makes it possible to determine the norms for the criterion parameters of IC reliability and estimate the permissibility of deviations in an operationally timely manner which have occurred during the fabrication of a specific batch of products. This in turn makes it possible to certify the technological process and subsequently make a judgement concerning the stability of the reliability level of the integrated circuits being produced based on the estimate of the stability of the production process for their fabrication.

A major tool for improving the quality and reliability of the IC's being produced is the continuous analysis of production process rejects, a comparison of the data obtained with the results of production tests (including technological) of the IC's and subsequent operationally timely correction of the conditions in those operations in the technological cycle which are responsible for the appearance of the defects ascertained in the output products. In this regard, it is exceptionally important to develop and implement methods of express quality control

for the operationally timely and objective estimation of process parameters as well as nondestructive quality control of semifinished products and finished IC's for the purpose of a timely determination and rejection of products with hidden defects. For this, it is essential to have automated high performance monitor and measurement equipment in all of the major operations of the technological cycle of IC fabrication.

The major methods of quality control (including nondestructive) used in IC production to measure the main parameters of individual components in their structure are given in [114-117, 124-126, 137, 138]. The great diversity of existing testing methods and the high requirements placed on the objectivity of the primary information and its operationally timely retrieval and processing, which are needed to assure control efficiency, as well as on the precision of the estimation of the quality level and the acceptable confidence level of integrated circuit reliability and quality prediction confront the designer and manufacturer of integrated circuits with a number of problems [125, 126].

First of all, there is the selection of the requisite system of parameters and characteristics to be monitored to provide for effective quality control. Since it is practically impossible to check all of the properties in all of the stages of IC production, it is necessary to select an optimal set of parameters and characteristics, which would make it possible with minimum expenditures for their measurement to assure the checking of the functioning of each IC under specific applications conditions, and test for hidden defects which lead to early failures or the degradation of the stability of IC properties with time.

In this case, it is exceptionally important to correctly determine the production process stages which are critical from the viewpoint of IC reliability, and based on this, to develop technically substantiated and effecient criteria for the rejection of potentially unreliable IC's during the stage of their fabrication.

This makes it possible to reduce the volume of quality control measurement and test operations to a minimum and to resolve the problem of optimizing the checking with respect to a specified quality level of the IC's as well as the expenditures to assure this.

Secondly, the volume of information needed for quality control increases significantly in step with an increasing level of integration and functional complexity of integrated circuits and the increase in the requirements placed on their quality and reliability.

The number of parameters of the production process, planar structures and finished IC's, which must be monitored during the manufacturing process, amounts to several hundreds when figured on a per integrated circuit basis. In this case, the complexity of the measurement techniques necessitates the use of special computer controlled data and instrumentation complexes for the testing. Since the primary information collected during the course of the testing should be processed in an operationally timely manner for the purpose of generating the correcting control actions, the range of computer applications will steadily expand in this sphere.

Thirdly, the problem of group prediction of the level of reliability and quality of IC batches fabricated on a certified production line using the basic production process takes on special importance. This is forecasting which is based on the computer processing of extensive quantities of information on the IC's and their structural components, collected during the process of manufacturing and subsequently testing the finished IC's, as well as special test structures. These data are supplemented by apriori information on the quality and reliability of the structural design and production process analogs of the IC's being checked (including the applications of IC's under actual conditions), utilizing knowledge of the mechanisms and quantitative characteristics of the degradation processes which occur in integrated circuits. Such forecasting makes it possible to eliminate or curtail the volume of a series of tests and obtain integrated circuits with a guaranteed level of quality and reliability.

At the present time, the following quality control techniques for testing between operations have proved out quite well and are widely used in integrated circuit production:

--Electrophysical methods (probe methods of measuring the parameters and characteristics of thin film and semiconductor elements and materials; measurement of the volt-ampere and volt-farad characteristics of circuits and components of IC's; removing and staining microscopic sectional slices, etc.);

--Optical methods (visual inspection, optical microscopy - including interferometry and a light scanning probe, etc.);

--Electron microscopy techniques (scanning electrol microscopy in various modes; X-ray microscopic analysis);

--Thermal methods (thermal resistance measurement, chemical heat indicators, etc.);

--X-ray techniques (radiography and X-ray television imaging);

--Leak detection techniques (mass spectrometry, bubble methods,etc.).

Additionally, new quality control techniques are being developed and introduced into production:

--Laser and holographic methods (laser ellipsometry, laser scanning, laser interferometry, holographic interferometry, etc.);

--Infrared techniques (IR interferometry, IR ellipsometry, IR radiometry);

--Liquid crystals;

--Acoustic noise methods and other techniques; (the specific features and capabilities of the major quality control methods indicated above are treated in § 6, and for this reason will not be cited here).

The development and implementation of new progressive methods of technical diagnostic work (including nondestructive testing methods) makes it possible to improve the efficiency of a quality control system even more for integrated circuits, given the state of the art in microelectronics.

With an increase in the functional complexity and level of integration of IC's, difficulties of quality control for finished IC's rise substantially: measurements of their electrical parameters, reliability tests and analysis of causes of their failures for the purpose of reliably determining structural components which have failed and defects in them responsible for the failure [27, 30, 32, 115, 144, 145]. From this point of view, the most promising method of improving testing and quality control efficiency, as well as estimating the reliability level of IC's is the concept of using test structures in all stages of IC planning and fabrication, a concept which has become widespread at the present time [74, 141-142].

We shall briefly treat the quality control system for integrated circuits during their production, based on the utilization of statistical monitoring of the technological process parameters and the characteristics of the IC's by means of test elements, structures and test "satellites". The wide scale use of test quality control methods makes it possible to maximally distribute the quality control operations over the entire technological process of manufacturing the integrated circuits.

It becomes possible in this case to substantially reduce the volume of the "output" quality control of finished IC's and the objectivity of the testing and the operational timeliness of the use of the obtained data in correcting the technological process are improved. Simultaneous with this, the utilization of quality control methods based on test elements, structures and check "satellites" substantially reduces the possibility of creating additional defects (cracks, dirt) in the "working" regions of the IC's, i.e., the product quality control technique is practically nondestructive.

A test structure takes the form of a specially designed chip, which incorporates various test elements, as a rule, not tied into the working circuits, and which make it possible to monitor the parameters of the physical structure of the IC for various values of the factors acting on the IC [28, 30, 32, 113, 140, 141-142, 152].

The listing of test elements of a test structure can include both elements of a special configuration intended only for estimating the parameters of the physical structure and their stability when subjected various loads, as well as actual components (bipolar and MOS transistors, diodes, resistors, etc.), employed in the IC's. The indicated elements can be provided in unit amounts or in the form of regular structures (circuits, blocks), figured in tens (or hundreds and thousands) of elements of the same type in one test structure, something which is necessary to estimate (or predict) the quantitative indicators of IC reliability based on the determination of the reliability indicators for the major structural components of the IC's.

The standard set of test elements, as a rule, incorporates:

a) Elements for checking the parameters of the physical structure:

--MOS capacitors in various oxide layers, intended for checking the oxide properties;

--Schottky diodes, etc.;

--MOS transistor of special configurations;

--Diffusion regions of special configurations, intended for checking the parameters of the diffusion processes and the characteristics of the planar structures;

--Tetrode transistor, which makes it possible to segregate the surface and body currents in a planar transistor, etc.;

b) Actual structural elements:

--Groups of bipolar and MOS transistors (working and "parasitic") of various geometries;

--Thin film conductors, contacts between conductors of different levels (in multilevel metallization) and other types of ohmic contacts of various configurations and geometric dimensions;

--Diffusion or deposited resistors;

--Elements of the interlevel insulation with various geometries;

--Working special purpose elements (for example, isolating diodes and other elements in the input circuits of the IC's to protect them against electrical overvoltages);

c) Elementary cells ("subblocks"), used as the basic logic gates of the IC's (especially for large scale integration).

In this case, the test structures can be arranged on each plate among the chips of "working" IC's (so-called test cells) or placed on separate plates, which go through the technological cycle at the same time as the "working" plates. During the testing, it is also permissible to use special test elements which are not tied into the working circuitry, or "working" circuits or elements of the IC which are accessible for measurements.

One of the possible test structure variants, which can also be used for testing the parameters of a physical structure (p-n junction doping depth, oxide thickness, etc.), including destructive testing techniques, are the so-called "satellite" plates ("witnesses"), which pass through the operations being monitored together with the "working" plates.

Yet another variant of test control is monitoring the mechanical strength of welded connections by the breakage method, which it is expedient to perform on "test" chips (which does not preclude the possibility of selective testing of the strength on the chips of "working" IC's, for example, those rejected because of their external appearance).

It must be especially underscored that a necessary condition for reliable quality control based on the utilization of any kind of structure (cells, elements, "satellites") is their fabrication in a single production process cycle with the main ("working") IC chips.

It is expedient to provide sets of elements of the same type (transistors, diodes, resistors, thin film conductors, etc.) which differ from each other only in the configuration and dimensions of the working regions, during the design stage of an IC, for the purpose of optimizing the characteristics of the structural components of the IC's (including the major circuit design elements) in the test structures.

The accumulation of test results for test structures with large numbers (hundreds and thousands) of IC elements of the same type in a wide range of electrical loads and environmental factors, as was noted above, makes it possible to estimate (predict) within a relatively short time (down to 1 year) the quantitative indicators for reliability which characterize the major structural design and production process variants of the integrated circuits. In this case, the tests themselves and the interpretation of the results obtained are substantially facilitated through the simplification of test equipment, measurement methods for test structures and the analysis of failed structural elements, something which makes it possible to simultaneously improve the confidence level of the results.

An important specific feature of IC reliability and quality testing methods using test structures is the comparative simplicity and considerable reliability in detecting and analyzing failed structural elements for the purpose of determining the causes and mechanisms of the failures, especially those related to group production process operations during IC fabrication. This obviously makes it possible to reduce the scope and duration of a number of technological tests, which as will be indicated below, are used for the purpose of stimulating hidden defects in IC's to ascertain and reject them.

The effectiveness of test quality control can be significantly improved, first of all, by means of designing and introducing, monitor, measurement and test equipment, specially intended for checking test structures, which should make it possible to put together sufficient statistics; secondly, by means of the wide scale utilization of computer processing techniques for the collected statistical data, which should make it possible to establish the correlation functions between the parameters of the technological process and the IC quality and reliability, determine the information carrying criterion parameters for the reliability, and in the final analysis, design a fully automated comprehensive production process control system for the manufacturing of IC's of a specified quality level based on the monitoring of test structures.

We shall once again turn to the control scheme for the production process of manufacturing IC's. Besides input quality control and testing between operations, there are also other forms of testing which are needed to guarantee a specified level of reliability for the output product:

--Production process tests and the rejection of defective products during production;

--Checking the quality and reliability, as well as the classification of good IC's with respect to the reliability level.

TABLE 21. The System of Production Process Testing and Rejection During the Production of Semiconductor Integrated Circuits

Kind of Production Process Test	Detected Integrated Circuit Defects												
	Structural imperfection in the semiconductor material	Damage to the chip surface	Disruption of the diffusion profile, photolithography and other defects which occur during chip fabrication	Scratches, breaks, cavities and porosity of thin film conductors and resistors	Surface contamination and the presence of foreign materials	Defects which occur in the chip during IC assembly	Defects in the welded contacts and wire conductors	Disruption of the hermetic seal of the IC package	Mismatching of the temperature coefficients of expansion of the materials	Defects in the IC package	Nonconformity of the electrical parameters to requirements of the standards documentation
Testing the electrophysical parameters during fabrication of IC chips	+	+	+		+						+
Testing the electrical parameters of the chips	+	+	+	+							+
Visual inspection of the chips		+	+	+	+						
Visual inspection of the IC bases prior to hermetic sealing		+	+	+	+	+	+			+	
High temperature treatment of the IC's	+	+	+	+			+	+	+		
Cycical exposure to a temperature change		+		+		+	+	+	+	+	

TABLE 21. [cont.]

Kind of Production Process Test	Detected Integrated Circuit Defects												
	Structural imperfection in the semiconductor material	Damage to the chip surface	Disruption of the diffusion profile, photolithography and other defects which occur during chip fabrication	Scratches, breaks, cavities and porosity of thin film conductors and resistors	Surface contamination and the presence of foreign materials	Defects which occur in the chip during IC assembly	Defects in the welded contacts and wire conductors	Disruption of the hermetic seal of the IC package	Mismatching of the temperature coefficients of expansion of the materials	Defects in the IC package	Nonconformity of the electrical parameters to requirements of the standards documentation
Exposure to linear loads (centrifuging)	+				+	+	+			+	
Testing the hermetic seal of the IC's								+			
Thermal and electrical conditioning of the IC's	+	+	+	+	+	+	+		+		
Final quality control of the electrical parameters of the IC's (in the range of ambient temperatures)	+	+	+	+	+	+	+				+
Visual inspection of the IC's								+		+	

A complex of production process tests occupies a special place among the measures which assure the output of high quality IC's. The major goal of these tests is to ascertain potentially unreliable IC's in a timely manner in the concluding stages of their fabrication. Additionally, information is obtained in this case which is needed to control the technological manufacturing process, since in this stage, it is comparatively easy to establish the correlation between the parameters of the technological process and typical kinds of production defects, and to determine the requisite corrective measures, directed towards the elimination of the ascertained sources of the defects.

Visual inspection of the chips and bases of the integrated circuits following mounting (prior to hermetic sealing) under a microscope is one of the most important rejection methods, since it makes it possible to detect in a timely manner numerous production defects which occur prior to the final operation of sealing the IC in the package. Typical defects which can remain unnoticed during the checking of the IC's for functioning and electrical testing of the integrated circuits, but which are revealed during visual inspection under a microscope (with a magnification of about 100x) are the following:

--Defects in thin film resistors and metal conductors (mechanical damage, defects in the photolithography - insufficient etching and overetching of conductors, corrosion, layer separation of the thin films, etc.);

--Defects in the oxidation and photolithography (local defects in the oxide, incorrect matching of the photographic templates, excessive etching or underetching of windows in the oxide close to the diffusion, the exposure of p-n junctions, etc.);

--Defects in scribing and separating the plates into chips (cracks and breaks in the chips, etc.);

--Improper fastening of the chip to the chip holder;

--Defects in the welded connections and wire leads (small welded contact area at the contact pads, adjacent wire leads which are impermissibly close to each other or welded contacts too close to the edge of the chip, mechanical damage to a wire, etc.);

--Contamination of the surfaces of a chip, leads, package components;

--The presence of foreign particles and other defects.

However, one must point out that the subjectivity of visual inspection, as well as the ambiguity of rejection criteria for some kinds of defects at times reduce the effectiveness of this type of quality control and necessitate, first of all, the refinement of existing methods of visual inspection for the purpose of improving the objectivity and confidence level of the inspection results, and secondly, the use of additional kinds of production process tests and rejections for the purpose of more reliable detection of IC's with production defects (especially hidden defects) [27, 145].

Technological tests include the following [27, 32, 36]:

--High temperature treatment of integrated circuits to stabilize their parameters;

--Thermal shock, thermal cycling, mechanical shock and centrifuging (or several of these effects) for the purpose of checking the immunity of the IC structural design to a cyclical change in the temperature or mechanical loading;

--Checking the hermetic seal of the IC's;

--Thermal and electrical conditioning of the IC's;

--Checking the electrical parameters of the IC's (including under extreme temperature values: the maximum and the minimum permissible in accordance with the technical specifications for the IC);

--Visual inspection of the IC's.

The system of IC technological testing is established as a function of their level of reliability which must be guaranteed. In accordance with the requirements of U.S. military standard MIL-STD-883, which has become widespread in foreign practice, the production of integrated circuits of a set level of reliability, as well as the sequence, composition and conditions for the production process tests are clearly regulated as a function of the class of IC reliability (A, B, C). Class A integrated circuits, in accordance with the definition of MIL-STD-883 are "devices intended for operation under conditions where repair or replacement of the components is extremely difficult or impossible, while reliability is of critical importance", i.e., in on-board space or aircraft radioelectronics equipment (REA).

Class B integrated circuits are intended for applications in radioelectronics equipment, although the repair of it is possible, it is difficult, and reliability is an important factor governing the operational indicators of the radioelectronics equipment.

Finally, Class C integrated circuits are characterized by a low level of reliability (as compared to Classes A and B) and are intended for applications in equipment, which can be repaired easily, while reliability does not play a great part.

The sequence and some of the conditions for the T5004 technological tests of MIL-STD-883 are indicated in Table 22 [32].

As can be seen from Table 22, a substantial increase is observed in the scope and degree of severity of the technological tests, in step with the increase in the requisite level of IC reliability.

The indicated types of technological tests are intended to ascertain hidden defects in integrated circuits, including those which occur during the process of hermetic sealing. In this case, the following major types of defects are detected:

--Contamination of the oxide film, surface of the chip and package components, which leads to instability in the IC parameters (primarily because of the appearance of inversion or ion leakage currents);

--Microholes in the dielectric films under thin film conductors of single and multiple level metallization;

--Unsatisfactory quality in covering the relief steps on the chip with metal;

--Poor ohmic contacts to the silicon ("metal to semiconductor") as well as between the thin film conductors of different levels (in multilevel metallization);

--Poor mechanical strength of the welded connections;

--Poor mechanical strength of the contact between the chip and the chip holder of the package;

--Unsatisfactory hermetic sealing of the welded and sealed seams and the glass insulators of the IC packages;

--Mechanical damage and corrosion of package components and other defects of the integrated circuits.

The indicated defects are usually not successfully detected during visual inspection and in the process of checking the electrical parameters of IC chips on the plate, since a more or less long time and rather high load levels are required to reveal them.

In chis regard, one of the most effective methods of technological testing is thermal and electrical conditioning which takes the form of IC testing during overall exposure to an elevated temperature and electrical loading, which simulates worst case conditions for IC application [27, 30, 32, 143, 148]. This

TABLE 22. The Sequence of Production Process Tests (Method T5004) for MIL-STD-883 as a Function of the Integrated Circuit Class

Kind of Test	Integrated Circuit Reliability Class A	B	C
Heat treatment to stabilize the parameters	24 hours	24 hours	24 hours
Thermal shock	15 cycles	15 cycles	15 cycles
Thermal cycling	10 cycles	or 10 cycles	or 10 cycles
Mechanical shock	20,000 g	--	--
Linear accelerations	30,000 g	30,000 g	20,000 g
Test of the hermetic seal	+	+	+
Exposure to critical electrical parameters	+	--	--
Thermal and electrical conditioning	168 hr + 72 hr	168hr	--
Final quality control of electrical parameters	+	+	+
X-ray testing	+	--	--
Exterior visual inspection	+	+	+

kind of testing makes it possible to ascertain the majority of the types of early ("burn-in") failures, such as:

--Elevated ion or inversion type leakage currents;

--Breakdowns of p-n junctions with hidden defects;

--Short circuits due to defects in the dielectric films;

--Short circuits of wire leads to each other and to the chip;

--Breaks due to mechanical damage or corrosion of the thin film components and flexible conductors, etc.

When selecting the optimum conditions for thermal and electrical conditioning, one must primarily be governed by the structural design and production process features of the integrated circuit as well as the specific kinds and mechanisms of failures inherent in the integrated circuits of the specific class (series or type).

TABLE 23. The Choice of Temperature and Electrical Modes for the Thermal and Electrical Conditioning of Integrated Circuits as a Function of the Dominant Kinds of Failures

Kind of IC Failure	Recommended Thermal and Electrical Conditioning Mode	
	T, °C	Electrical Mode
Elevated leakage currents (because of the formation of inversion channels)	> 100	Static mode (the feeding of as low a potential as possible to the p-type bases)
Short circuits of the wire leads to each other and to the edge of the chip	T_{max} (in accordance with standards documentation)	Static mode (feeding the maximum potential to the leads relative to the IC substrate)
Breakage of thin film conductors (because of burnout in local thin places)	T_{max} (in accordance with standards documentation)	Static mode (feeding forward bias to the maximum number of p-n junctions: the maximum permissible current flow). Dynamic mode (for IC's, the power dissipation of which depends substantially on the switching frequency).
Corrosion (chemical and electrochemical) of the metal and resistive films with the action of contaminants	50-90	Static mode (feeding the maximum permissible positive potential to the IC leads)
Breakdown of a p-n junction (because of hidden defects)	T_{max} (in accordance with standards documentation)	Static mode (feeding the maximum permissible reverse bias to the maximum number of p-n junctions).
Short circuit in the dielectric film		

The most effective conditions, which make it possible to ascertain defects leading to the failures indicated above, are shown in Table 23, which was compiled on the basis of generalizing the materials of testing, operating and the results of analyzing failures and studies of mechanisms of the typical IC failures [30, 40, 147-149].

In order for the conditioning to be effective, it is essential to carefully think through and work out the procedure for these tests. Thus, for example, in the case where the presence of two or more fundamentally different failure types or mechanisms is characteristic of an integrated circuit of a specific series (or type), where different temperature and electrical conditions are required to ascertain these types or mechanisms, it is expendient to employ a "combination mode" of IC thermal and electrical conditioning, i.e., to perform the given production process testing in several stages with changing conditions.

Researchers working with LSI MOS integrated circuits [30] also note that the existing differences of opinion concerning which conditions for thermal and electrical conditioning are more effective for such integrated circuits (static or dynamic conditions), have no firm ground to stand on, since neither of these tests make it possible to stimulate numerous kinds of failures, because of the fact that the majority of LSI integrated circuit components cannot be loaded in the corresponding manner.

There is as yet no single point of view concerning the duration of thermal and electrical conditioning. In the U.S. military standard MIL-STD-883 for integrated circuit testing methods, various durations of thermal and electrical conditioning are recommended, right up to 250 hours [32, 36, 150]. At the same time, according to different sources [32, 149, 143, 148], up to 90 to 95% of all IC failures which can be ascertained by thermal and electrical conditioning are observed during the first 100 to 168 hours, and by the 168'th hour, rejects reach an almost constant level.

The average percentage of defective integrated circuits which can be detected during thermal and electrical conditioning amounts to 2.6 to 5% of the total number, although depending on the IC manufacturer, this percentage can fluctuate from batch to batch in the wide range of from 0 to 20% [30, 39, 143].

Detecting the indicated 90 to 95% of potentially unreliable integrated circuits makes it possible to reduce the failure rate of IC's during their subsequent operation by approximately 1.5 to 2 orders of magnitude [149, 150, 143]. However, according to the data of paper [143], the cost of integrated circuits which have undergone thermal and electrical conditioning, and certain other kinds of expensive technological testing, increased by a factor of about 50 times, while the delivery timeframes increased by a factor of 2 to 3 times. In this case, about 25% of the number of IC's which failed during operation were acknowledged as potentially unreliable, but were not ascertained during rejection testing because of its inadequate effectiveness. This example clearly illustrates how relative the estimate of production process and rejection testing is and how important it is to compare the additional costs incurred by rejection testing with the "cost" of IC failure during subsequent operation [27, 32, 144].

According to the latest data, the cost of 168 hour electrical conditioning of integrated circuits performed by the company using the integrated circuits following their input quality control can be significantly reduced: down to 5 cents per IC [143], however, as before, this kind of testing remains extremely labor intensive and expensive, comprising the bulk (about 30 to 40%) of the outlays for technological testing and rejection of integrated circuits [32]. The necessity of making a careful economic analysis for the purpose of determining the permissible percentage of defective devices in delivered batches of IC's is obvious from this.

TABLE 24.

Integrated Circuit Reliability or Cost Indicator	Integrated Circuit Class				With Special Checking (Selection)
	Industrial	C	B	A	
Failure rate, $x10^{-8}$ hr^{-1}	30-100	10-50	3-8	2-5	1
Relative IC cost	1.0	1.3	1.8	2.8	4-6

An estimate of the cost of technological testing, which has been made by several foreign IC manufacturers [27, 32, 149, 143], makes it possible to approximately determine the level of expenditures for IC reliability assurance (without considering the outlays for improving the structural design and fabrication technology of the integrated circuits). Generalized data for a comparison of the relative costs of IC's with their guaranteed reliability level are presented in Table 24 as a function of the volume of the technological tests.

In order to correctly estimate the true effectiveness of measures to assure IC reliability, and in particular, the effectiveness of technological testing and rejection of potentially unreliable IC's during their production, it is necessary to analyze the costs of increasing IC reliability as part of a whole with the analysis of the cost of possible IC failure during various stages of its application.

TABLE 25. Comparison of the Costs of Detecting and Removing Defective Integrated Circuits in Various Stages of Their Application for Four Classes of Electronic Systems

Class of Electronic System (Area of Radioelectronic Equipment Application)	Cost of IC Failure at Various Stages of IC Use, $$			
	During Input Quality Control of the IC's	During Assembly of Electronic Equipment Units	During System Tests	Under Operational Conditions
General purpose	2	5	15	50
Industrial use	4	25	45	215
Military	7	50	120	1,000
Space	15	75	300	200 million

A governing factor in this regard is the cost of detection of defective integrated circuits by the customer during input quality control or when they are ascertained during the installation and alignment of units, system testing or under conditions of equipment operation. The costs of detecting and removing defective integrated circuits in the indicated stages of their application are compared in Table 25 [27, 144] for four classes of electronic systems (according to function): general use, industrial service, military and space hardware.

It can be seen from this Table, for example, that a space system manufacturer can allow himself 15 times the outlays in hardware as compared to a manufacturer of general use equipment for the practical prevention of IC failures during the stage of installing the units. In later stages of the application, this difference becomes even more pronounced.

Attention should be drawn to the fact that besides the economic expediency in the determination of the optimal system of technological tests and in the selection of their conditions (the load levels), it is essential to also work from considerations of guaranteeing the preservation of the nondefective integrated circuits. It is well known that some kinds of tests (thermal shock, mechanical shock, etc.) are service life tests in a number of cases. Unjustifiedly rigorous conditions for the performance of such tests incorporated in the rejection (or technological) testing can lead to the opposite effect: to the exhaustion and a reduction in the reliability of the "conditioned" IC's [37].

In conclusion, the exceptional importance of a comprehensive approach to the problem of reliability assurance for integrated circuits during their fabrication must be underscored. Just check and rejection operations alone do not allow for attaining high IC reliability indicators, especially for LSI integrated circuits, if there is no unified effective control system for the technological process, which operates on the basis of a systematic development and realization of the corrective measures to eliminate ascertained sources of failures, as well as a system for continually improving the IC designs.

10. Reliability Assurance for Integrated Circuits in Their Applications Stage

As practice demonstrates, the incorrect application of integrated circuits is one of the major sources of their failures. According to existing data [27, 32, 34, 35], IC failures during the process of installing, debugging and operating radioelectronic equipment complexes are related to the incorrect choice of their operational modes, and violations of the requirements of the standards setting documentation. For this reason, reliability assurance for integrated circuits during operation consists in the correctness of their application. Properly designed radioelectronic circuitry will always meet the requirements of high reliability. For this, there are various means available to the designer to achieve the optimum circuit design solutions.

The following are numbered among the major methods of increasing the reliability of radioelectronic equipment using integrated circuits:

--Designing the radioelectronic equipment, taking into account the maximum easing of the operation modes of the IC's incorporated in it;

--Selecting a radioelectronic equipment fabrication technology which prevents impermissible effects from acting on the integrated circuits during their installation in units, adjustment and technological testing ("run-ins") of the radioelectronic equipment assemblies and units;

--Additional hermetic sealing of the radioelectronic equipment or its individual units (assemblies) to prevent the exposure of the IC's to elevated humidity, contaminants, corrosive environments, sea fog and other undesirable environmental factors.

From the viewpoint of easing the operating modes, it is quite important to reduce the temperature at the integrated circuit chip for the purpose of minimizing temperature dependent failure mechanisms which reduce the reliability. It is expedient for this to reduce the ambient temperature in radioelectronic equipment units as much as possible and to provide for the use of power IC's with heat sinks.

It is promising during the equipment design stage to limit the maximum electrical loads on the IC's and to take special steps to protect the IC's against current and voltage overloads, which can occur during radioelectronic equipment fabrication and operation.

The choice of the manufacturing technology for radioelectronic equipment should also be based on considerations of preventing factors from acting on the IC's which are not provided by the standard setting engineering documentation (excessive mechanical loads, the use unrecommended methods of fastening and mounting integrated circuits on circuit boards, washing mixtures, which have a harmful effect on the IC's, etc.).

Moreover, it is necessary to make provisions for special measures directed towards protecting integrated circuits against static electricity discharges during their installation and subsequent operation as part of radioelectronic equipment.

TABLE 26.

$P_{on.}(t)$	$S=\frac{\ln P_{вепх}(t)}{\ln P_{on.}(t)}$		
	2	5	10
0,9	0.81	0,59	0.34
0,99	0,98	0,95	0.90

To maintain integrated circuit reliability indicators at the level necessary for the construction of highly reliable radioelectronic equipment, one must in every way avoid using IC's under combination load conditions, which have an extremely unfavorable impact on their reliability (for example, simultaneous exposure to an electrical load and the maximum permissible temperature and ambient humidity).

Of no small importance in assuring the reliability of radioelectronic equipment designed around integrated circuits is information on IC reliability, which is taken into account in the calculation of equipment reliability. Using understated reliability indicators in this case complicates the task of designing equipment with the requisite level of reliability to a considerable extent. The calculation of radioelectronic equipment reliability based on $P_{верх}$ [P_{upper}] with a confidence level of P* substantially understates the reliability [151]. Values of the upper confidence limit for the probability of nonfailure operation, P_{upper}, at P* = 0.95 are given in Table 26 for several trial values of the probability of nonfailure operation, $P_{оп}$, as a function of the relationship: $S = [\ln P_{upper}(t)]/[\ln P_{trial}(t)]$. The difference between P_{upper} and P_{trial} can reach an order of magnitude and more. In this case, the calculated reliability level proves to be greatly understated. Thus, using operational indicators for integrated circuit reliability in calculations of the reliability of radioelectronic equipment is the most correct approach which assures an objective estimate of the anticipated reliability of the equipment.

CHAPTER VI. Metrological Support for Integrated Circuit Reliability and Quality Control

11. The Role and Place of Metrological Support in the Quality Control System

Ways of assuring integrated circuit reliability were treated above. The list of them would be incomplete and the plans for improving reliability of little effect if metrological support for quality control was not included in them.

Integrated circuit fabrication quality basically depends on the state of production process discipline during production and the implementation of the installed technology. Effective monitoring of the observance of the technological process of integrated circuit manufacture assures the timely rejection of defective units from the aggregate of manufactured IC's. Quality control precision plays a decisive part in this case.

As follows from the preceding sections, very stringent requirements are placed on quality control facilities. In order to exclude errors in estimating the values of the IC parameters being monitored, improve the confidence level of test results, achieve uniformity in the methods monitoring and evaluating reliability, and consequently also reproducibility of the quality control results, it is essential to have timely metrological supports for the measurements and tests.

Metrological support is one of the functions of a quality control system. This function is directed towards assuring unity, precision and reliability of product quality measurements [167, 186].

Metrological support for the economy is understood to be the "Establishment and application of the scientific and organizational principles, technical hardware, rules and norms essential for attaining unity in the requisite precision of the measurements", in accordance with GOST 1.25--76 "State Standardization System. Metrological Support. Basic Principles".

The scientific foundation of metrological supports is metrology: the science of measurements, as well as the methods and means of assuring their unity and the requisite precision. The equipment basis of metrological support is comprised of the systems for assuring unity in the measurements, state reference standards, etc. The organizational basis for metrological support is the USSR Metrological Service.

The effective performance of metrological support functions by a comprehensive product control system makes it possible to reduce rejection losses, improve the quality of the output product, increase the yield on capital and the utilization factor for scientific equipment and production equipment, as well as achieve maximum uniformity in quality evaluation and lay down the conditions governing the other components of labor efficiency [186].

12. Basic Principles of Metrological Support for Integrated Circuit Reliability and Quality Control

Integrated circuit quality control consists in checking for the conformity of the properties of IC quality to the requirements of the engineering standard setting documentation and is composed of measurements, tests and alternative criterion monitoring. The latter is distinguished from measurements in that during quality control by this method, the fact that the quantity being measured falls within a specified tolerance range is established with a definite confidence level. Measuring the quantity provies for establishing its numerical value with a certain error.

The means of integrated circuit quality control are measurement tools (meters, transducers, as well as measurement installations, systems and auxiliary equipment), test facilities (test complexes and systems, chambers, test stands, machines, instruments and installations as well as auxiliary test facilities) and quality control hardware (flaw detectors, displays, gauges, quality control sorting machines).

The metrological support for integrated circuit quality control (also including reliability) consists in establishing the scientific and organizational bases for the testing, selection as well as the setting up and utilization of the hardware, regulations and norms needed to achieve a reliable estimate (within a specified precision) for the conformity of the product quality indicators being monitored to the established requirements for the assured unity of the measurements and tests.

Metrological support for quality control is accomplished by means of setting standards for the listing of quantities being monitored, precision standards for the measurements and the reproducibility of the test conditions, the methods and conditions for the measurements and tests as well as methods of estimating measurement error, the metrological characteristics of the measurement and the test hardware, the classes of precision of the measurement hardware, the technical requirements placed on the methods and means of metrological supervision of the instrumentation and test equipment, and the methods of quality control and estimating the reliability of quality control facilities.

Another form of metrological support for quality control is the design and correct utilization of the calibration base as well as the selection and setting up of the quality control facilities which meet the requirements governed by standards.

It is difficult to hypothesize the attainability of measurement and test unity without certification of the methods and facilities for quality control including for the subdivisions and specialists engaged in this work. For this reason, certification of the procedures for the performing measurements, test techniques, as well as metrological and test services and centers is yet another very important form of metrological support for quality control.

And finally, the last of the most important forms of the activity considered here of industrial enterprises and metrological and test services is the state inspectorate and departmental supervision of the observance of standards and technical specifications, as well as of the implementation of the metrological rules and the

status, application and reliability of quality control facilities (including state tests of measurement and test facilities).

The precision and unity of quality control, which correspond to the requirements of the technical documentation, are attainable given the condition that the adopted units for physical quantities are used and uniformity is assured in the quality control by the use of standard terminology, classification and reference data on the properties of substances and materials.

Considerable basic literature has been written concerning the methods and means of providing for precision and unity in measurements and quality control. The contents of metrological support for various kinds of measurements are being constantly published in the pages of the journals IZMERITAL'NAYA TEKHNIKA [INSTRUMENTATION ENGINEERING], METROLOGIYA [METROLOGY] and METROLOGIYA I TOCHNYYE IZMERENIYA [METROLOGY AND PRECISION MEASUREMENTS]. For this reason, without repeating the general principles, we shall consider the specific features inherent in integrated circuit production which are responsible for the requirements placed on the metrological support for the production of these products, and determine its contents, standards and organization.

It is more difficult to provide for measurement unity in microelectronics in other sectors of the economy. The specific features of metrological support for the production of semiconductor integrated circuits are expressed primarily in the very high requirements placed on the ranges and precision of the measurement of integrated circuit parameters (they are practically comparable to reference standards) as compared to other sectors of industry, as well as the high requirements placed on the quality of the materials, semi-finished products and product packages and the increased requirements on the precision with which the fabrication technology is observed.

Practically all of the existing kinds of measurements find application in integrated circuit production. Moreover, a large number of specific measurements not used in otherfields of science and engineering are employed in microelectronics. These are measurements of the rate of growth, weight and thickness of a film, the surface of quality of a film, the type of conductivity, the specific resistance of a semiconductor material and the distribution of doping impurities in the body of a semiconductor, as well as the volt-ampere and volt-farad characteristics of p-n junctions, voltage and current levels, pulse delays and widths, the frequency, phase and nonlinear distrotion of signals, etc.

The necessity of careful operational quality control in the manufacture of integrated circuits and control of the production process is dictated by the distinctive features of the production of microelectronic devices of this class, the major ones of which are the great labor intensity of integrated circuit fabrication (there are 30 to 40 major operations counted in just the technological process of IC manufacture alone) and the necessity of assuring practically defect free production in each operation. It is indicated in [4] that to obtain a yield of 30 percent good integrated circuits, a good product output of no less than 97 percent must be achieved in each operation.

The most important condition for obtaining a high percentage yield of high quality IC's is the purity of the environment, the materials and work positions. Without effective monitoring of the purity of the materials used and the ambient medium in each technology operation, the attaining of the requisite production indicators is unthinkable: labor productivity and production economy; the specified quality and reliability of the output products also prove the unattainable.

To manufacture high quality integrated circuits, it is necessary in a number of cases to use silicon with a specific resistance on the order of 10 to 100 ohm · cm.

Water occupies an important place in IC production. Water of a high degree of purity is used for these purposes. Deionized water, having a resistance of 10 to 20 Mohm is considered satisfactory.

Gases occupy a no less important place in integrated circuit production.

The tolerances for the IC parameters employed in the course of the production process have a substantial impact on the percentage yield of integrated circuits.

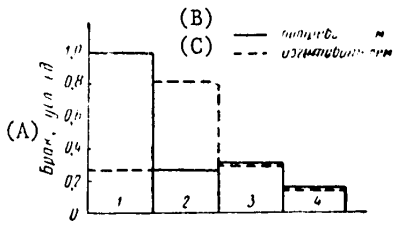

Figure 32. Distribution of rejects as a function of reasons for rejection.

Key: 1. Electrical parameter;
2. Breakage of contact connections;
3. External appearance;
4. Other.

A. Rejects, relative units.
B. By the customer;
C. By the manufacturer.

It can be seen from an analysis of the typical distributions of the values of the resistances of diffusion resistors in a single IC that a tolerance on the nominal value of +10% provides for a resistor yield of 56%, and with a tolerance of ±5%, the yield is 30% [4]. This in turn places very stringent requirements on the precision with which the geometric dimensions and parameters of the physical structure of the diffusion resistors are observed. Moreover, dimensional effects in the region of the ohmic contacts of thin film conductors to the diffusion resistors of the integrated circuit should be carefully taken into account. Thus, for example, the contact resistance of thin film resistors should be minimal and not exceed 2 to 10 ohms for an area of 625 μm^2. A resistor 25 μm wide is fabricated with a permissible deviation not exceeding five percent, which means it is necessary during the process of monitoring the geometric dimensions of the resistors to provide for the measurement of quantities of down to one micrometer.

The reproducibility of resistors is assured by the reproducibility of the surface resistance of deposited films. During the deposition of a film, its resistance is continuously monitored. The requirements provide for a precision in the reproduction of the surface resistance of films of less than one percent along a plate and two percent from plate to plate.

When fabricating capacitors of the metal--oxide--semiconductor type, the thickness of the oxide dielectric is monitored, which fall in a range of 50 to 100 nm. The capacitance of such capacitors amounts to 320 to 640 pF/mm^2.

The inductance in integrated circuits varies from 0.1 μHy at quality factors ranging from 1 to 10.

A maximum total deviation in the dimensions of no more than 5.5 μm is permitted during the photolithography process. These include: the tolerance for the original of 0.6 μm; the permissible deviation during multiplication of $\pm$ 1.2 μm; the precision in processing the photoresist of 1.2 μm and errors in matching the photographic templates of 2.5 μm.

These are only a few of the examples which characterize the requirements placed on measurement precision in the production of semiconductor IC's. The requirements placed on measurement facilities used for quality control in integrated circuit fabrication during their manufacture are governed not only what has been presented above. The microminiature dimensions of integrated circuits place unusually stringent requirements on the contact and hook-up assemblies of measurement hardware. Thus, for example, the probes of measurement equipment should make contact with the surface being studied through a hole in the oxide layer on the order of 12 · 12 μm. For this, the point of the probe should have a radius not exceeding 5 μm, while the spacing between adjacent probes should not exceed 50 μm.

The mass nature of the production of the product considered here requires not only precise, but also rapid measurement of the parameters. In order for the rate at which the measurements are performed not to slow down the rate of growth in labor productivity in microelectronics, measurement hardware should have a high operational speed.

The limited possibilities of using general purpose standardized instrumentation in microelectronics are responsible for the necessity of designing of special measurement gear. In this case, its design should even run somewhat ahead of the development of new types of integrated circuits.

The incessant growth in the products list of semiconductor materials used for the fabrication of new types of integrated circuits and the practically incessant process of improving their manufacturing technology makes it difficult to provide modern measurement methods and hardware in a timely manner for production, which meet the requirements of the engineering standards setting documentation.

A great deal of work has been done in recent years which is directed towards accelerating the pace of development of meterological support for the national economy and microelectronics in particular. The reference standard base has been strengthened, the precision of numerous reference standards has been improved and

the ranges of the quantities which can be measured have been extended; the creation of a state service of standard samples and a state service of standard reference data for the properties of substances and materials has been started; new prototypes of high precision instrumentation have been designed. The system of territorial organs of the State Standards Administration and departmental services has been further expanded. Along with this, there are still serious defiencies in this most important work in the microelectronics sector of industry which are holding up further progress. There are practically no prototype units for a number of the most important kinds of measurements or the requisite meterological base. A serious obstacle to further improving the precision and reliability of measurements is the lack of certain standard samples of semiconductor materials.

The lag in the meterological support for measurements in semiconductor microelectronics generates violations of the meterological regulations and a failure to observe the approach to the design of quality control facilities established by the standards. Among the most frequently encountered violations of general meterological requirements are those which are due to the failure to resolve procedural questions of certifying new quality control hardware. The negative consequences of such a situation are exacerbated by the widescale use of equivalents in integrated circuit quality control. Load simulators, which themselves should be checked and calibrated with a periodicity of up to two to three times per work shift.

Providing for measurement unity under these conditions proves to be extremely difficult. The doubtful reliability of the measurement results then impedes the further development of this most important sector of the economy.

Improving the level of integrated circuit quality control is substantially retarded by the failure to understand the role of meterological support for quality control tests in the system of quality control meterological support. Moreover, the quality control test facilities, along with the measurement hardware, play the part of quantitative quality control facilities. We shall consider the meterological aspects of testing, taking into account the fact that this question of quality control is not well worked out.

Integrated circuit quality consists of properties which characterize functional capabilities, which segregate it from a number of similar ones, as well as properties which govern the operational possiblities. The physical quantities which characterize the functional properties of integrated circuits are practically all measured by means of measurement facilities. The majority of the operational properties of IC quality cannot be measured directly. The reliability of integrated circuits, heat, moisture, cold and vibrational immunity, as well as certain properties of the quality are determined by means of test facilities, which create physical fields in the space surrounding the product being tested, causing definite structural or physical and chemical transformations in the objects being studied, and by means of the built-in measurement hardware, make it possible to estimate with the requisite precision the response of the integrated circuit to the perturbing forces and the conformity of circuit's operational properties to the requirements of the engineering standard settind documentation.

The tests of [101] are broken down into research and quality control tests. The former are performed for the purpose of studying the possibility of producing the

requisite properties in the integrated circuits, while the second are performed for quality control. Depending on the problem being solved, the test operation has the nature of a research study, or serves as a means of establishing with a certain error the numerical value of the quantity being monitored. In the latter case, the test operation is similar to the measurement operation. In the process of testing for reliability, non-failure operating time, shelf-life, moisture immunity and operational stability in the presence of moisture as well as immunity to solar radiation and fog, fungal resistance and other tests, values of the physical quantities or their derivatives with respect to time are determined. For example, IC reliability is defined for operation in a definite electrical mode and ambient conditions by the number of failures per unit time. Approximately the same thing can be said about operational stability during vibration and similar quality properties, which characterize the capability of the product of performing its function in the presence of external perturbations. All of them, strictly speaking are estimated in terms of the number of failures over a definite period of exposure to the perturbing force, or at each power level of the force, i.e., during the testing of the product. This indicates the active role of test equipment in estimating the property of quality. Test facilities not only generate the external effects with which the tested unit is brought to the state needed to solve the measurement problem (for example, resonace of IC elements when estimating vibration immunity, activating the major and minority carries when estimating thermal stability), but also the given quality property of the product is estimated by means of the measurement hardware either directly or indirectly.

In order to bring the product to the requisite state, in other words artificially reproduce conditions close to operational ones, the testing facilities reproduce the physical fields in the space surrounding the unit being tested. If one takes into account the fact that measurement instrument measure the size of the physical quantity only at one point in space and only for one of the vectors of the applied load, then it is easy to come to the conclusion that testing is the only method of quantitatively estimating those properties of product quality which characterize its ability to stand up to the destructive effect of the resulting forces composed of several force vectors acting in the ambient space. During quality control tests of a product, the testing facilities which reproduce the standardized exposure levels for the test object play a joint role with the measurement gear: in the form of quality control facility. The problem of assuring unity of the tests is more complex than the problem of assuring unity of the measurements, since the metrological support for the tests incorporates the assurance of precision and unity of the tests as well as adequacy of the test facilities in addition to the metrological support for the measurements [186].

In speaking of the unity of tests, we shall have in mind the uniformity of the methods of performing the tests, the monitoring of test modes as well as recording and evaluating the results obtained taking into account the fact that errors in setting and maintaining the test conditions, and measuring and recording the results are known within definite confidence limits and fall within the range of the specified tolerances.

We shall term those test facilities adequate, the standardized metrological characteristics of which, having an influence on the test precision, conform to the set requirements throughout the entire duration of the test, while the assigned measurement facilities are graduated in legallly stipulated units and maintain their metrological properties constant during the testing period.

Testing precision is assured by the optimal setting of standards for the listing of the test mode parameters being monitored as well as the requirements placed on the precision of setting and maintaining the test conditions, the methods of monitoring the test parameters, the implementation of the standardized mode, as well as the adequacy of the testing facilities. Setting the standards for that enumerated above is accomplished on the basis of an analysis of requirements placed on the quality of the products being tested and the requirements placed on the precision of the tests, the design of the test unit and the known physical failures and laws governing their occurrence as well as the development and timewise distribution with respect to the type of load exposure.

Unity of the tests is assured by the following: the selection and establishing of the derivatives of the units of the quantities employed for the test mode characteristics; establishing the kind of effect, the sequence for their realization and the standards (range of test loads and duration of exposure); the designation and providing of identical test conditions for products of the same type; suitability for the use of the test facility and test results; by the state insepctorate and departmental quality control for the implentation of the standards and the technical specifications for the test methods and facilities.

The adequacy of test facilities is achieved by establishing and setting standards for the precision characteristics of the test facilities which have a direct impact on testing precision, as well as the requirements placed on the methods and facilities of the metrological inspectorate of testing equipment, the requirements placed on testing facilities, the regulations and standards for test equipment design, the methods and facilities for certification and checking test machines, chambers, stands and instruments; and methods of calculating reliability. It is natural that in addition to setting standards for that enumerated above, the performance of state tests for standardized and metrological certification of nonstandardized test facilities, as well as the state supervision and departmental control of the status, application and reliability of testing equipment during operation is quite important in assuring the adequacy of test facilities.

The following serve as the most important standardized metrological or precision characteristics of test facilities: the precision in setting the physical quantity--test mode parameter (FV-PIR) [PQ-TMP], the permissible deviation from the standardized value of the PQ-TMP, the error in maintaining the PQ-TMP and the nonuniformity in the distribution of the PQ-TMP being reproduced by the test facility. The standard concept "setting precision" is understood to be the precision in reproducing the PQ-TMP, specified by the engineering standard setting documentation. In other words, the precision in setting in the PQ-TMP is the difference between the values of the specified PQ-TMP and that reproduced by the test equipment while the error in maintaining the PQ-TMP is the deviation in the actual value of the physical quantity, which characterizes the test mode, from the specified value during the testing process. The permissible deviation from the standardized value is the

difference between the physical quantity at the control point and at any other point on the test platform (the useful volume) of the test stand or machine (chamber), while the nonuniformity in the distribution of the PQ-TMP is the difference between the maximum and minimum values of the reproduced physical quantity, measured at any two points in the useful volume of the chamber or test stand (or machine) platform at any point in time [186].

The priority task of metrological support for integrated circuit reliability and quality control is improving the reliability of the tests. This problem is being solved successfully with the introduction of automated quality control systems. These systems make it possible to increase the confidence level of quality control results while substantially reducing the volume of check operations and curtailing the quality control labor intensity. Automated test control systems (ASUI) have already been introduced and are successfully functioning, which control the operation of five climatic chambers for 56 days practically without the participation of an operator. Automated test control systems provide for maintaining the specified test conditions in the chambers, shutting them down at the exspiration of the preprogrammed time or in the case of breakdown. The systems are designed around information and control computers.

The task of metrological support for quality control using nondestructive techniques comes up as one of the priority problems at the present time.

Presently, nondestructive quality control facilities are practically not at all subjected to metrological supervision. In the better case, just as in the case of test facilities, they are checked, calibrated and certified by their owners. In this case, different owners use different methods, which do not agree. If one adds to what has been said that fact that certification is accomplished using only working measurement tools, while new samples of nondestructive quality control equipment as a rule, are not subjected to state tests [105], the pointlessness of attempts to assure the precision, reliability and unity of quality control using nondestructive methods becomes obvious without the implementation of state metrological supervision and departmental metrological monitoring.

It is necessary to standardize the methods for state metrological inspection and departmental metrological quality control of the technical condition of nondestructive quality control equipment during the operational process. The development of new hardware for nondestructive quality control of integrated circuits should be accomplished with the participation of the metrological scientific research institutions of the State Standards Administration, and their production should be sanctioned by the State Standards Administration.

13. State Supervision and Departmental Monitoring of Metrological Support

In conclusion, we shall consider the procedure for implementing state supervision and departmental monitoring of metrological production support.

The procedure for implementing state supervision of metrological production support for a product is regulated by the "Temporary Procedural Instructions for the

Implementation of State Supervision of Metrological Production Support for a Product"*. This document is published as a supplement to the "Instructions for State Supervision of the Implementation and Observance of Standards and Technical Specifications". It governs the procedure for preparing and performing checks of metrological support for the production of a product, where these are accomplished in the process of state metrological inspection, as well as the rules for completing the forms for these check results.

A new form of state supervision of measurement equipment is expert evaluation of the reliability of measurement facilities.

Expert evaluation of reliability is accomplished in accordance with MU 8.8-77 [Procedural Instructions 8.8-77] "Procedural Instructions for the Performance of Expert Examination of Measurement Facility Reliability", which were worked out in developing the standards for the State Standardization System and the State System of Measurement Unity Assurance. This document defines the tasks of expert examination of measurement facility reliability, the procedure for presenting them for the expert examination and the performance of this work, and sets the overall technical requirements placed on the formating of the results obtained.

Various organs of state and departmental metrological services perform expert evaluations of the reliability of measurement instruments, systems and complexes. During expert metrological evaluation of the engineering assignments for the development of master and very important working measurement facilities, this problem is solved by the metrological institutes and the metrology and standardization centers of the State Standards Administration. They render the expert evaluation of the reliability when analyzing the materials of state acceptance tests for measurement equipment, as well as state quality control tests if these tests are performed in connection with the end of the period of validity of production authorization for measurement equipment. In the other instances of performance of the state quality control tests, this inspection function is formed by the territorial organs of the State Standards Administration.

The metrological services of the head and base organizations of the ministries and departments are engaged in the expert evaluation of reliability in the stage of rendering expert metrological opinions on the technical assignments for the development of measurement equipment.

In the stage of state acceptance tests for measurement facilities, the expert evaluation of reliability is made in accordance with the authorized technical assignment for the development of the measurement equipment and the draft of the technical specifications. In this case, the calculations of product reliability or the materials of the definitive reliability tests are analyzed and the project plans for the quality control test procedure for reliability testing are analyzed as well as the charts for the technical level and quality of the product and the operational documentation provided by GOST 2.601-68 "YeSKD. Operational Documents".

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*Moscow, Izdatel'stvo Standartov, 1974.

In contrast to the case considered here, during state quality control tests of measurement facilities, the expert evaluation of the reliability is made in accordance with the approved documents: the technical specifications for the product, the procedure for the reliability quality control tests, tests and the chart for the technical level and product quality. In this case, the materials of reliability tests of previous state or quality control tests, as well as operational documentation are also considered.

Among the technical documentation in accordance with which the expert evaluation of the reliability is made, there can be other documents which contain information on the reliability of the object subject to expert evaluation.

The steps in the work are covered by the procedure. In the first of them, the presented materials are checked for conformity to reliability requirements provided by the valid state standards and other standard setting documents. Based on the results of analyzing the presented materials, an evaluation is made of the correctness of the selected listing and standardized values of the reliability indicators. At the same time, conformity to the periodicity of the metrological servicing of the measurement facilities to the standardized values for metrological reliability indicators is assessed.

The reliability calculation is evaluated in subsequent stages in the process of rendering the expert evaluation of the reliability during state acceptance tests, while in the process of acceptance and quality control tests, the substantiation of the procedure for reliability quality control tests is analyzed.

The correctness of the confirmation of the reliability indicators by the reliability test results and by other methods is evaluated in the concluding step.

The results of the expert reliability evaluation, when rendering the expert metrological opinion on the technical assignments for the development of measurement facilities, are set forth in the expert conclusion. In the case of state quality control tests, they are reflected in a document of the commission, while when considering the materials of state tests, in a general conclusion drawn up in accordance with MU 8.2-71, which governs the procedure for formating and analyzing the materials with the results of state tests of measurement facilities.

14. Centralization of Tests: a Way of Improving the Level of Metrological Support for Quality Control

The development of testing subdivisions in industrial enterprises up to a level which provides for the performance of the complete set of tests called for in the standard setting documentation in step with the further increase in the requirements placed on product quality and the increasing complexity of testing methods caused by this is becoming economically disadvantageous. Along with the appearance of new types of tests, techniques and equipment for their performance, the products list of test equipment is growing as well as the complexity of testing facilities, the production space set aside for the tests and the consumption of all kinds of energy and materials. In the majority of cases, the revision of

methods and standard programs for tests is accompanied by an increase in the duration and cost of the tests. For some kinds of products, the length of tests increases by several times. Thus, for example, the testing time for the American "Tiros" earth satellites amounts to 50 percent of the time expended on their construction. As a result, the enormous material resources are deflected away from the production of the product to quality control. Testing expenses in machine building amount to 10 to 15 percent of the overall outlays for the construction of a product. In electrical engineering production, they reach 30 percent, while in semiconductor production and microelectronics, they even reach 80 percent. The funds which could have been used to implement measures directly targeted at improving the quality of the output product are expended in evaluating its quality.

The expenditures are not always justified in this case. In a number of cases, funds are expended for testing, the low confidence level of which is known beforehand. In the production process, quality control techniques are frequently introduced which can be counted amoung superfluous testing. In this case, cases of product failure which have successfully passed all of the tests are not at all uncommon in practice.

If we add to what has been pointed out here that in this case, the load on design organizations and plants producing the test facilities, increases at the same time, then the picture is complete.

One of the real ways of resolving the contradictions indicated here is the centralization tests.

Concentrating the requisite equipment and personnel in specialized test centers, transfering a number of organizational functions and quality control for the output product to them which are now performed by various base organizations for metrology, standardization and product applications, as well as by industrial enterprises, will assure attaining obvious advantages. One of the most important results of centralization will be a unified approach to the evaluation of the quality of the products being tested, and as a consequence, an improvement in the confidence level of the assessment. The level of scientific research and trial design work will increase substantially in the field of testing methods and hardware. The quality of the development of standards and governing technical materials for the requirements placed on tests and methods of their performance, the standards and rules for metrological supervision as well as techniques of evaluating the results obtained will increase. Their will be a real possibility of automating work on the development of testing programs, controlling the tests, recording and analyzing the data on the quality of the products being tested using computer equipment. The demand for custom made test equipment will fall off sharply and some difficulties will be eliminated in and of themselves which are due to the lack of testing facilities and the necessity of expanding their production. It will become possible to concentrate skilled test personnel and to improve the level of their training.

And finally, as a result of test centralization, favorable conditions will be created for the formation of a technical policy in the field of standardizing requirements placed on quality control and testing methods.

As a result, material expenditures for product quality control will be reduced by many times. Industrial enterprises, freed from the performance of tasks not natural to them, will be able free a portion of the production areas and personnel engaged in testing for the needs of production, and to concentrate their efforts and equipment on the working out and refinement of the production processes and the design of the output products. The conditions for assuring the unity of the tests will improve immeasurably.

The most expedient form for centralization of tests is combining small, low capacity testing subdivisions and enterprises and the creation of state, intersectoral and sectoral testing centers.

The economic justification for the design, placement and construction of test centers, their specialization and the scope of their work should all be treated primarily from the viewpoint of economic expediency.

Minimal expenditures for testing and transporting the products being tested with minimal timeframes for the execution of the work should be used as the criterion of the economic efficiency of test centralization.

A calculation of the economic efficiency of test centralization within the framework of a scientific production association in one of our domestic microelectronics industry sectors shows that as a result of centralization, the annual profits can be figured in hundreds of millions of rubles [178].

BIBLIOGRAPHY

1. Kolosov A.A., et al., "Poluprovodnikovyye tverdyye skhemy" ["Hard Semiconductor Circuits"], Moscow, Sovetskoye Radio Publishers, 1965.

2. "Mikroelektronika" ["Microelectronics"], Edited by N.P. Bogoroditskiy, Moscow, Sovetskoye Radio Publishers, 1965.

3. Valiyev K.A., et al., "Elektronnaya Tekhnika. Ser. VI. Mikroelektronika" ["Electronic Engineering. Series 6. Microelectronics"], 1967, No. 6.

4. Madland G.R., et al., "Integral'nyye skhemy. Osnovy proyektirovaniya i tekhnologii" ["Integrated Circuits. Design and Technology Fundamentals"], Translated from the English, Edited by A.A. Kolosov, Moscow, Sovetskoye Radio Publishers, 1968.

5. "Integral'nyye skhemy. Printsipy konstruirovaniya i proizvodstvo" ["Integrated Circuits. Design and Productions Principles"], Translated from the English, Edited by A.A. Kolosov, Moscow, Sovetskoye Radio Publishers, 1968.

6. Valiyev K.A., et al., "Tsifrovyye integral'nyye skhemy na MDP transistorakh" ["Digital Integrated Circuits using MOS Transistors"], Moscow, Sovetskoye Radio Publishers, 1971.

7. Gavrilov R.A., Skvortsov A.M., "Tekhnologiya proizvodstva poluprovodnikovykh priborov" ["Semiconductor Device Production Technology"], Leningrad, Energiya Publishers, 1968.

8. TRUDY INSTITUTA INZHENEROV PO ELEKTROTEKHNIKE I RADIOELEKTRONIKE [PROCEEDINGS OF THE IEEE (in translation)], Moscow, 1969, No. 57, p 9.

9. Hoeneisen B., Mead C., SOLID STATE ELECTRONICS, 1972, Vol. 15, No. 8.

10. Al'tman, ELEKTRONIKA [ELECTRONICS], 1974, Vol. 47, No. 4.

11. Al'tman, ELEKTRONIKA, 1975, Vol. 48, No. 14.

12. Khorton, et al., ELEKTRONIKA, 1975, Vol. 48, No. 3.

13. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA [FOREIGN ELECTRONICS ENGINEERING], 1974, No.5.

14. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA, 1974, No. 10.

15. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA, 1974, No. 3.

16. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA, 1975, No. 6.

17. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA, 1973, No. 7.

18. "Miniatyurizatsiya i mikrominiatyurizatsiya radioelektronnoy apparatury" ["Miniaturization and Microminiaturization of Radio Electronic Equipment"], Edited by N.A. Barkanov and I.S. Likhachev, Moscow, Mir Publishers, 1965.

19. Prangishvili I.V., et al., "Mikroelektronika i odnorodnyye struktury dlya postroyeniya logicheskikh vychislitel'nykh ustroystv" ["Microelectronics and Homogeneous Structures for the Construction of Computer Logic Devices"], Moscow, Nauka Publishers, 1967.

20. Lennon J., "An Analysis of Potential Avionic Reliability Improvement Through Microelectronics", Wescon Technical Papers, 1964, Vol. 2.

21. Moskovitz C., "Integrated Circuits in Action. Part 3.", ELECTRONICS, 1966, Vol. 39, No. 26.

22. Bumgart V.F., et al., "Obzor materialov mezhdunarodnogo kongressa IEEE, 1965" ["Review of Materials from the 1965 International Congress of the IEEE"], RADIOELEKTRONIKA ZA RUBEZHOM [RADIOELECTRONICS ABROAD], 1965, No. 27-28.

23. "Status Report of Integrated Circuits Reliability", "Microelectronics and Reliability", 1965, Vol. 4.

24. Bridges J., "Integrated Electronics in Defense System", PROCEEDINGS OF THE IEEE, 1964, Vol. 52, No. 12.

25. "Proceedings of the 12th National Symposium on Reliability and Quality Control", 1966, 25-27th Jan.

26. "The Seventh Annual New York Conference on Electronic Reliability, 1966", 25 - 27th, Jan.

27. Pitti S.G., "Slagayemyye nadezhnosti poluprovodnikovykh priborov" ["The Components of Semiconductor Device Reliability"], PROCEEDINGS OF THE IEEE, 1964, Vol 62, No 2.

28. Pek D.S., et al, "Nadezhnost' poluprovodnikovykh priborov na firme Bell System" ["Semiconductor Device Reliability in the Bell System"], PROCEEDINGS OF THE IEEE, 1974, Vol 62, No 2.

29. Heitornwhite R.F., et al, "Obespecheniye postavok vysokonadezhnykh poluprovodnikovykh komponentov" ["Assuring Deliveries of High Reliability Semiconductor Components"], PROCEEDINGS OF THE IEEE, 1974, Vol 62, No 2.

30. Colburn Ye.D., et al., "Nadezhnost' MOP BIS" ["MOS LSI Reliability"], PROCEEDINGS OF THE IEEE, 1974, Vol 62, No 2.

31. Synorov V.F., et al., "Fizicheskiye osnovy nadezhnosti integral'nykh skhem" ["The Physical Principles of Integrated Circuit Reliability"], Edited by Yu.G. Miller, Moscow, Sovetskoye Radio Publishers, 1976.

32. Vakkaro I.V., "Trebovaniya k nadezhnosti poluprovodnikovykh priborov pred'yavlyayemyye Ministerstvom oborony SShA" ["Requirements Placed on the Reliability of Semiconductor Devices by the U.S. Defense Department"], PROCEEDINGS OF THE IEEE, 1974, Vol. 62, No. 2.

33. Khamiter, ELEKTRONIKA [ELECTRONICS], 1969, Vol 42, No 13.

34. Saito M., et al., REVIEW ELECTRIC COMMUNICATIONS LABS, 1973, Vol 5, No 5-6.

35. ELECTRONIK ZEITUNG [ELECTRONICS NEWS], 1975, Vol 4, No 7, p 34.

36. Brauer J.B., MICROELECTRONICS, 1969, June, p 17.

37. Gallo M.D., SAE PREPRINT, s.a. N 710798.

38. Fuqua N., RAC Internal Memor., 1972.

39. Nowak T.J., in "Proc. 1967 Annual Symp. Rel."

40. Hausrath D.A., Fleming D.C., in "Proc. 1968 Annual Symp. Rel."

41. Matare G., "Elektronika defektov v poluprovodnikakh" ["The Electronics of Defects in Semiconductors"], Moscow, Mir Publishers, 1974.

42. Aleksandrov L.N., "Kinetika obrazovaniya i struktury tverdykh sloyev" ["The Structure and Formation Kinetics of Hard Layers"], Novosibirsk, 1972.

43. Plantinga H., IEEE TRANSACTIONS ON RELIABILITY, 1969, Vol. ED-16, No 4.

44. Seligson, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

45. D'Orl', "Tekhnologiya tolstykh i tonkikh plenok" ["Thin and Thick Film Technology"], Moscow, Mir Publishers, 1972.

46. Blake, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

47. Balk, Eldridge, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

48. Shneybl, Kin, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

49. Browing G.V., et al., "Phys. Failure Electron.", 1966, Vol 4.

50. A. [sic], "Failure Mechanism of Gold-Aluminum Integrated Circuit Bonds", WESCON TECHNICAL PAPERS, 1965, Vol 65, No 9.

51. Cunningham J.A., SOLID STATE ELECTRONICS, 1965, Vol 8, No 8.

52. Philofsky E., SOLID STATE ELECTRONICS, 1970, Vol 13, No 10.

53. Berger W.M., et al., PHYS. FAILURE ELECTRON, 1966, Vol 4.

54. Rossiter T.J., in "Ninth Annual Proc. Reliab. Phys. Symp.", 1971.

55. Philofsky E., in "Ninth Annual Proc. Reliab. Symp." [sic], 1971.

56. Hakim E.B., Malinovsky G., in "11th Annual Peoc. Reliab. Phys. Symposium", 1973.

57. Edfors H.C., In "Proc. 1972 Annual Reliability and Maintainability Symposium, 1972".

58. Terri, Wilson, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

59. ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA [FOREIGN ELECTRONICS ENGINEERING], Special Issue.

60. Black J.R., IEEE TRANS., 1970, Vol ED-17, No 9.

61. Joseph R.R., et al., in "Eighth Annual Proc. Reliab. Phys. Symp." 1970.

62. Schlacter, M., et al., IEEE JOURNAL SOLID STATE CIRCUITS, 1971, SC-6, No 5.

63. Hazarov I.N., et al, "Elektronnaya tekhnika. Ser. 3, Mikroelektronika" ["Electronics Engineering. Series 3. Microelectronics"], 1975, No 1.

64. Metts, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

65. Andre, et al., "Composants electron haute fiabilite" [sic] ["High Reliability Electronic Components"], Colloq. Int. Toulouse (1972), 1972.

66. Brandewie G.V., et al., PHYS. FAILURE ELECTRON., 1966, Vol 4.

67. Paulson W.M., in "11th Annual Proc. Reliab. Phys. Symp., 1973".

68. Clough W.L., Collins J.M., MICROELECTRONICS, 1973, Vol 3, No 11.

69. Satake I., et al., JAPAN JOURNAL APPL. PHYS., 1973, Vol 12, No 4.

70. Devaney J.R., in "Eighth Annual Proceedings Reliability Phys. Symp. 1970".

71. Black J.R., IEEE TRANSACTIONS, 1969, Vol ED-16, No 4.

72. Spitzer S.M., Schwartz S., IEEE TRANSACTIONS, 1969, Vol ED-16.

73. Santoro, Tolliver, "Tekhnologiya tolstykh i tonkikh plenok" ["Thin and Thick Film Technology"], Moscow, Mir Publishers, 1972.

74. Prabhakar G.B., et al., IEEE TRANSACTIONS 1973, R-22, No 4.

75. SOLID STATE ELECTRONICS, 1973, Vol 16, No 12, p 1399.

76. JOURNAL OF ELECTROCHEMICAL SOCIETY, 1973, Vol 120, No 4, p 521.

77. ELECTRON. DESIGN, 1973, Vol 21, No 6, p 54.

78. Schlegel E.S., et al., in "Eighth Annual Proc. Reliab. Phys. Symp., 1970".

79. Grey, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

80. Schlegel E.S., Schnable G.L., IEEE TRANS., 1969, Vol ED-16, No 4.

81. Goryunov N.N., "Svoystva poluprovodnikovykh priborov pri dlitel'noy rabote i khranenii" ["The Properties of Semiconductor Devices During Long Term Operation and Storage"], Moscow, Energiya Publishers, 1970.

82. Atalla M., et al., BELL SYSTEM TECHN. JOURNAL, 1959, No 3.

83. Schlacter M.M., et al., IEEE TRANSACTIONS, 1970, Vol ED-17.

84. Krigler R.J., Deveny T.F., in "11th Annual Proceedings Reliability Physical Symposium, 1973" [sic], p 153.

85. Eccleston W., Pepper M., MICROELECTRONICS AND RELIABILITY, 1971, No 10.

86. Attardo M.J., Rosenberg R., JOURNAL OF APPLIED PHYSICS, 1976, No 41.

87. White, "Tekhnologiya tolstykh i tonkikh plenok" ["Thin and Thick Film Technology"], Moscow, Mir Publishers, 1972.

88. Kaverznev V.A., et al., "Staticheskoye elektrichestvo v poluprovodnikovoy promyshlennosti" ["Static Electricity in the Semiconductor Industry"], Moscow, Energiya Publishers, 1975

89. Kostychev G.I., MIKROELEKTRONIKA [MICROELECTRONICS], 1971, No 4.

90. Berg H., et al, in "11th Annual Proc. Reliab. Phys. Symp., 1973".

91. Yefimov I.Ye., Kal'man I.G., "K voprosu otsenki kachestva i nadezhnosti integral'nykh tverdykh skhem" ["On the Question of Estimating the Quality and Reliability of Hard Integrated Circuits"], ELEKTRONNAYA TEKHNIKA. SER. IV, [ELECTRONICS ENGINEERING, SERIES 4], 1967, No 6.

92. Yefimov I.Ye., Kal'man I.G., "Ob odnov storone problemy nadezhnosti poluprovodnikovykh integral'nykh skhem" ["On One Aspect of the Problem of Semiconductor Integrated Circuit Reliability"], in the book, "Sb. Nauch. trudov po problemam mikroelektroniki" ["Collected Scientific Papers on Problems in Microelectronics"], MIET [Moscow Institute of Electrical Engineering], 1968.

93. GOST 8.054-73 GSI: Metrologicheskoye obespecheniye podgotovki proizvodstva. Obshchiye polozheniya" ["State Standard 8.054-73 GSI: Metrological Support for Production Preparations. General Principles"].

94. GOST 8.010-72. GSI: "Obshchiye trebovaniya k standartizatsii i attestatsii metodik vypolneniya izmereniy" ["General Requirements Placed on the Standardization and Certification of Measurement Performance Procedures"].

95. "Obespecheniye nadezhnosti poluprovodnikovykh ustroystv" ["Reliability Assurance for Semiconductor Devices"], Edited by A.S. Savina, Moscow, Mir Publishers, 1964.

96. Kouden D., "Statisticheskiye metody kontrolya kachestva" ["Statistical Quality Control Methods"], Edited by B.R. Levin, Moscow Fizmatgiz Publishers, 1961.

97. Shor Ya.B., "Statisticheskiye metody analiza i kontrolya kachestva i nadezhnosti" ["Statistical Methods of Reliability Quality Control and Analysis"], Moscow, Sovetskoye Radio Publishers, 1962.

98. Kalabro S., "Printsipy i prakticheskiye voprosy nadeshnosti" ["Principles and Practical Questions in Reliability"], Edited by D.Yu. Panov, Moscow, Mashinostroyeniye Publishers,, 1966.

99. Ponomarev V.P., Frolov L.N., "Rol' avtomatizirovannoy sistemy upravleniya ispytaniyami pri kontrole izdeliy elektronnoy tekhniki v protsesse proizvodstva" ["The Role of an Automated Testing Control System in Checking Electronic Products During the Production Process"], ELEKTRONNAYA TEKHNIKA. SER. 8, 1974, No 7 (25).

100. GOST 13377-67: Nadezhnost' v tekhnike. Terminy. ["State Standard 13377-67: Reliability in Engineering. Terms"].

101. GOST 16504-74:Kachestvo produktsii. Kontrol' i ispytaniya. Osnovnyye terminy i opredeleniya" ["State Standard 16504-74: Product Quality. Monitoring and Tests. Main Terms and Definitions"].

102. Kal'man I.G., Kovalenko A.S., Kurnikov I.B., "K voprosu ekonomicheskoy otsenki effektivnosti trenifovki izdeliy na nadezhnost'" ["On the Question of an Economical Estimate of the Efficiency of Reliability Conditioning of Products"], NADEZHNOST' I KONTROL' KACHESTVA [RELIABILITY AND QUALITY CONTROL], 1971, No 1.

103. GOST 15467-70: Kachestvo produktsii. Terminy. [State Standard 15467: Product Quality. Terms].

104. GOST 16962-71. Izdeliya elektronnoy tekhniki i elektrotekhniki. Mekhanicheskiye i klimaticheskiye vozdeystviya. Trebovaniya i metody ispytaniy [State Standard 16962-71: Electronic Equipment and Electrical Engineering Products. Mechanical and Climatic Loads. Testing Requirements and Methods].

105. GOST 8.001-71. GSI: Gosudarstvennyye ispytaniya sredstv izmereniy [State Standard 8.001-71. GSI: State Tests of Measurement Facilities].

106. Reese I., "Reliability Prediction for Monolithic Integrated Circuits", ARINC Res. Corp., Publ. No. 947-01-1-1143, 1971, Nov.

107. Kal'man I.G., "Vozdeystviye faktorov vneshney sredy na apparaturu i elementy" ["The Effect of Environmental Factors on Equipment and Components"], "Metody klimaticheskikh i mekhanicheskikh ispytaniy" ["Climatic and Mechanical Testing Methods"], Moscow, Znaniye Publishers, 1971.

108. Petrovskiy A.A., Yesyutin A.A., "Organizatsiya ispytaniy na vozdeystviye klimaticheskikh faktorov" ["Setting Up Tests for Exposure to Climatic Factors"], IZMERITEL'NAYA TEKHNIKA [INSTRUMENTATION ENGINEERING], 1975, No 5.

109. Dammer A., Griffin B., "Ispytaniye radioelektronnoy apparatury i materialov na vozdeystviye klimaticheskikh i mekhanicheskikh usloviy" ["Testing Radio Electronic Equipment and Materials for the Effect of Climatic and Mechanical Conditions"], Moscow-Leningrad, Energiya Publishers, 1965.

110. Malinskiy V.D., "Kontrol' i ispytaniya radioapparatury" ["Monitoring and Testing Radio Equipment"], Moscow, Energiya Publishers, 1970.

111. GOST 9763-67: Pribory elektronnyye izmeritel'nyye. Obshchiye tekhnicheskiye trebovaniya [State Standard 9763-67: Electronic Measurement Instruments. General Technical Requirements].

112. Pushkarev G.I., Rettel' A.I., Gorodetskaya N.K., "Zamena udarnykh ispytaniy ispytaniyami na lineynyye peregruzki" ["Substituting Linear Overloads for Shock Load Tests"], IZMERITEL'NAYA TEKHNIKA, 1975, No 5.

113. ELECTRONICS, 1971, No 9.

114. Dokuchayev Yu.P. et al., ELEKTRONNAYA PROMYSHLENNOST', 1972, No 7.

115. Grigor'yan V.G., ELEKTRONNAYA PROMYSHLENNOST', 1972, No 7.

116. Makmagon, ELEKTRONIKA [ELECTRONICS], 1971, Vol 44, No 8.

117. Fistul' V.I., et al., ELEKTRONNAYA PROMYSHLENNOST' [ELECTRONICS INDUSTRY], 1972, No 7.

118. Harris L.A., JOURNAL OF APPLIED PHYSICS, 1968, Vol 39.

119. Shinoda G., et al., in "Proc. Sixth Int. Conf. X-Ray Optics and Microanalysis" Osaka, Japan, 1971.

120. Thornton P.R., et al., IEEE TRANS. ELECTRON DEVICES, 1969, Vol ED-16.

121. Beaulier R.P., et al, in "Proc. 10th Annual IEEE Reliab. Phys. Symp.", Las Vegas, 1972, p 32.

122. Behera S.K., et al. [sic].

123. Electronics, 1972, No 2. [sic].

124. Rabodzey N.V., Lyubimov Ye.M., ELEKTRONNAYA PROMYSHLENNOST', 1972, No 7.

125. "Fiziko-tekhnicheskiye metody nerazrushayushchego kontrolya elementov i priborov elektronnoy tekhniki" ["Technical-Physical Methods of Nondestructive Testing of Electronic Equipment Components and Devices"], in the book, "Sb. Nauchno-tekhnicheskogo Obshchestva radioelektroniki i svyazi imeni Popova" ["Collected Papers of the Scientific and Technical Society for Radio Electronics and Communications imeni Popov"], Moscow, 1969.

126. Proleyko V.M., ELEKTRONNAYA PROMYSHLENNOST', 1972, No 7.

127. Schaft H.A., in "11th Annual Proc. Reliab. Phys. Symp., 1973".

128. Brauer J.B., et al., in "Eighth Annual Proc. Reliab. Phys. Symp., 1970".

129. Gianelle W.H., PHYS. FAILURE ELECTRON., 1966, Vol 4.

130. Lepselter M.P., BELL SYSTEM TECHN. JOURNAL, 1966, Vol 45.

131. Eleftherion M.P., WESTERN ELECTRON. ENG., 1967, Vol 11, No 4..

132. Grossman, ELEKTRONIKA, 1974, Vol 47, No 10.

133. Skrupski, ELEKTRONIKA, 1971, Vol 44, No 3.

134. Skrupski, ELEKTRONIKA, 1971, Vol 44, No 8.

135. White G., in "11th Annual Proc. Reliab. Phys. Symp., 1973, p. 94.

136. Bullis, Skeys, PROCEEDINGS OF THE IEEE, 1969, Vol 57, No 9.

137. Amazaspyan V.N., et al., ELEKTRONNAYA PROMYSHLENNOST', 1972, No 7.

138. Kontsevoy Yu.A., Kudin V.D., "Metody kontrolya tekhnologii proizvodstva poluprovodnikovykh priborov" ["Production Technology Quality Control Techniques for Semiconductor Devices"], Moscow, Energiya Publishers, 1973.

139. Reynolds, et al., PROCEEDINGS OF THE IEEE, 1974, Vol 62, No 2.

140. Pinon T., "Composants electron. haute fiabilite [sic]" ["High Reliability Electronic Components"], Colloq. Int. Toulouse (1972), Paris, 1972.

141. Nazar'yan A.R., et al., ELEKTRONNAYA TEKHNIKA. SER. 3. MIKROELEKTRONIKA [ELECTRONICS ENGINEERING. SERIES 3. MICROELECTRONICS], 1972, No 1.

142. Karmazinskiy A.N., MIKROELEKTRONIKA, 1974, No 7.

143. Lorandzher, ELEKTRONIKA, 1975, Vol 48, No 2.

144. Danner, Lombardy, ELEKTRONIKA, 1971, Vol 44, No 18.

145. Schoonard J.W., et al., ERGONOMICS, 1973, Vol 16, No 4.

146. Miranda, ELEKTRONIKA, 1968, Vol 41, No 17.

147. Brown G., "11th Annual Proc. Phys. Symp., 1973".

148. Kemeny A.P., MICROELECTRONICS AND RELIABILITY, 1974, Vol 13, No 2.

149. Barber D.E., O'Connel E.P., "NATO Conference on Reliability Testing and Reliability Evaluation", Hague, 1972.

151. Shor Ya.B., "Statisticheskiye metody kontrolya kachestva i nadezhnosti promyshlennoy produktsii" ["Statistical Reliability and Quality Control Techniques for Industrial Products"], Materials from lectures given in the Polytechnical Museum in a semina on reliability and progressive product quality control methods, Moscow, Znaniye Publishers, 1968.

150. Brauer J.B., ELECTRON PRODUCTS, 1969, August.

152. Kkhambata A., "Bol'shiye integral'nyye skhemy" ["Large Scale Integrated Circuits"], Moscow, Mir Publishers, 1971.

153. GOST 1845-59: Pribory elektroizmeritel'nyye. Obshchiye tekhnicheskiye trebovaniya [State Standard 1845-59: Electrical Measurement Instruments. General Technical Requirements].

154. GOST 8.002-71. GSI: Organizatsiya i poryadok provedeniya poverki, revizii i ekspertizy sredstva izmereniy [State Standard 8.002-71. GSI: The Organization of and Procedure for Testing, Modifying and Rendering Expert Evaluations of Measurement Facilities].

155. GOST 8.054-73. GSI. Metrologicheskoye obespecheniye podgotovki proizvodstva. Obshchiye polozheniya [State Standard 8.054-73. GSI. Metrological Support for Production Preparations. General Principles].

156. Arapenkov A.P., et al., "Ispytaniya i poverka kontrol'no-izmeritel'nogo oborudovaniya dlya proizvodstva integral'nykh skhem" ["Testing and Calibration of Quality Control and Measurement Equipment for Integrated Circuit Production"], METROLOGIYA [METROLOGY], 1973, No 10.

157. "Metrologicheskiye sluzhby ministerstv i vedomstv. Tipovyye polozheniya. RDTP 54-75--RDTP 57-75" ["Metrological Services of Ministries and Departments. Standard Regulations RDTP 54-75--RDTP 57-75"], Moscow, Izdatel'stvo Standartov, 1975.

158. Arapenkov A.P., Bogoroditskiy P.A., Bondarevskiy A.S., "Nekotoryye voprosy metrologicheskogo obespecheniya kontrol'no-izmeritel'nogo oborudovaniya dlya IS" ["Some Questions of Metrological Support of the Quality Control and Instrumentation Equipment for Integrated Circuits"], ELEKTRONNAYA PROMYSHLENNOST' [ELECTRONICS INDUSTRY], 1973, No 4.

159. Kal'man I.G., "Metrologicheskaya attestatsiya ispytatelnogo oborudovaniya i kachestvo produktsii" ["Metrological Certification of Test Equipment and Product Quality"], STANDARTY I KACHESTVO [STANDARDS AND QUALITY], 1974, No 3.

160. Kipnis A.M., "O nadzore za ispytatel'noy tekhnikoy" ["On the Inspection of Test Equipment"], IZMERITEL'NAYA TEKHNIKA [INSTRUMENTATION ENGINEERING], 1975, No 5.

161. Popov V.V., Chepaykin V.A., "O proyekte GOST 'Metrologicheskiy nadzor za sredstvami ispytaniy. Organizatsiya i poryadok provedeniya'" ["On the State Standards Draft: 'Metrological Inspection of Testing Facilities. Organization and Procedure for Implementation'"], IZMERITEL'NAYA TEKHNIKA, 1975, No 5.

162. Frolov L.N., "Nekotoryye zadachi tekhnicheskogo obsluzhivaniya sredstv izmereniy i kontrolya parametrov izdeliy elektronnoy tekhniki" ["Some Problems of Technical Servicing of Parameter Monitoring and Measurement Facilities for Electronic Equipment Products"], ELEKTRONNAYA TEKHNIKA. Ser. 8, 1975, No 3 (33).

163. Vasil'yev Ye.A., Frolov L.N., "Sostavlyayushchiye metodicheskoy pogreshnosti izmereniya dinamicheskikh parametrov integral'nykh mikroskhem" ["Components of the Procedural Error in the Measurement of the Dynamic Parameters of Integrated Circuits"], ELEKTRONNAYA TEKHNIKA. SER. 8, 1974, No 6 (24).

164. "Vremennyye metodicheskiye ukazaniya o poryadke gosudarstvennogo nadzor za metrologicheskim obespecheniyem porizvodstva produktsii" ["Temporary Procedural Instructions on the Procedure for Inspection of the Metrological Support for Product Manufacture"], Moscow, Izdatel'stvo Standartov, 1974.

165. "Instruktsiya po gosudarstvennomu nadzoru za vnedreniyem i soblyudeniyem standartov i tekhnicheskikh usloviy. RDI1-72" ["Instructions for the State Inspection of the Introduction and Observance of Standards and Technical Specifications. RDI1-72"], Moscow, Izdatel'stvo Standartov, 1972.

166. Mardin V.V., et al., "Gosudarstvennyye ispytaniya - osnova povysheniya kachestva vypuskayemoy produktsii"["State Tests: The Basis for Improving Output Product Quality"], IZMERITEL"NAYA TEKHNIKA, 1975, No 6.

167. "Kompleksnaya sistema upravleniya kachestvom produktsii. Rekomendatsii po razrabotke i vnedreniyu v ob"yedineniyakh i na predpriyatiyakh" ["The Comprehensive Product Quality Control System. Recommendations for Development and Introduction in Associations and Enterprises"], Moscow, Izdatel'stvo Standartov, 1976.

168. Zaks A.M., Malykh V.A., Mif N.P., "Metrologicheskoye obespecheniye tekhnologicheskoy podgotovki proizvodstva" ["Metrological Support of the Technological Preparation for Production"], IZMERITEL'NAYA TEKHNIKA [INSTRUMENTATION ENGINEERING], 1973, No 4.

169. Rekomendatsii po postroyeniyu i funktsionirovaniyu sistemy gosudarstvennogo upravleniya kachestvom produktsii na baze standartizatsii (kontseptsiya i osnovnyye polozheniya) ["Recommendations for the Design and Functioning of the State Product Quality Control System Based on Standardization (Concept and Basic Principles)"], Moscow, VNIIS [All-Union Scientific Research Institute for Standardization], 1975.

170. Kruglov M.I., Kryzhanovskiy I.D., Golant M.Ye., "Organizatsiya rabot po sozdaniyu yedinoy sistemy gosudarstvennogo upravleniya kachestvom produktsii" ["The Organization of Work on the Creation of the Unified System of State Product Quality Control"], STANDARTY I KACHESTVO [STANDARDS AND QUALITY], 1976, No 1.

171. Lebedev G.I., "Metrologicheskoye obespecheniye proizvodstva v sisteme upravleniya kachestvom" ["Metrological Support for Production in a Quality Control System"], IZMERITEL'NAYA TEKHNIKA, 1976, No 6.

172. Mallin U.R., "Avtomatizatsiya metrologicheskogo obespecheniya upravleniya kachestvom" ["Automating the Metrological Support for Quality Control"], IZMERITEL'NAYA TEKHNIKA, 1976, No 6.

173. Golovashkin M.A., Mikhaylenko V.D., Mif N.P., Shkabardnya M.S., "Metrologicheskoye obespecheniye priborostroyeniya" ["Metrological Support for Instrument Making"], IZMERITEL'NAYA TEKHNIKA, 1975, No 10.

174. Kiparenko V.I., Zaks L.M, Mif N.P., "Razvitiye standartizatsii v oblasti metrologicheskogo obespecheniya narodnogo khozyaystva" ["The Development of Standardization in the Area of Metrological Support for the Economy"], IZMERITEL'NAYA TEKHNIKA, 1975, No 9.

175. "Osnovy standartizatsii i kontrolya kachestva" ["Fundamentals of Standardization and Quality Control"], Edited by V.V. Tkachenko, Moscow, Izdatel'stvo Standartov, 1973.

176. GOST 1.1-68. GSS: Organy i sluzhby standartizatsii ["State Standard 1.1-68. GSS: Standardization Organs and Services"].

177. Kal'man I.G., Martynov G.K., "Povysheniye effektivnosti kontrolya kachestva" ["Increasing Quality Control Efficiency"], STANDARTY I KACHESTVO, 1973, No 2.

178. Kal'man I.G., "Ekonomicheskaya effektivnost' tsentralizatsii ispytaniy promyshlennoy produktsii" ["The Economic Effectiveness of Centralizing Testing of Industrial Products"], METROLOGY, 1975, No 9.

179. Donde Yu.Ya., "Metrologicheskaya sluzhba i kontrol' kachestva produktsii" ["The Metrological Service and Product Quality Control"], IZMERITEL'NAYA TEKHNIKA, 1971, No 3.

180. Malikov I.M., Zaydenberg M.G., "Spravochnik inzhenera-ispytatelya sudovoy elektroradioapparatura" ["Handbook for the Marine Electrical and Radio Equipment Testing Engineer"], Leningrad, Sudostroyeniye Publishers, 1976.

181. Kiparenko V.I., Popov V.V., "O metrologicheskom nadzore za ispytatel'noy tekhnikoy" ["On the Metrological Inspection of Test Equipment"], IZMERITEL'NAYA TEKHNIKA, 1973, No 9.

182. Donde Yu.Ya., "Organizatsiya metrologicheskogo nadzora za izmeritel'nym i ispytatel'nym oborudovaniyem" ["The Organization of Metrological Inspection of Measurement and Test Equipment"], IZMERITEL'NAYA TEKHNIKA, 1974, No 9.

183. Kizim V.D., "O nadzore za ispytatel'noy tekhnikoy" ["On the Inspection of Test Equipment"], IZMERITEL'NAYA TEKHNIKA, 1972, No 4.

184. Kotlyarov V.I., "Opyt raboty metrologicheskoy attestatsii sredstv ispytaniy v Estonskoy SSR" ["Operational Experience with Metrological Certification of Testing Facilities in the Estonian Soviet Socialist Republic"], IZMERITEL'NAYA TEKHNIKA, 1974, No 3.

185. Ivlev A.I., Zaks L.M., "Sovremennyye printsipy razvitiya sistemy metrologicheskogo obespecheniya narodnogo khozyaystva" ["Modern Principles of the Development of the System of Metrological Support for the Economy"], IZMERITEL'NAYA TEKHNIKA, 1973, No 4.

186. Kal'man I.G., "Osnovy metrologicheskogo obespecheniya kontrolya kachestva produktsii priborostroyeniya" ["Principles of Metrological Support for Product Quality Control in Instrument Making"], Moscow, Znaniye Publishers, 1979.

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